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Time Domain and Statistical Model Development, Simulation and Correlation Methods for High Speed SerDes

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Abstract

IBIS Algorithmic Modeling Interface (IBIS-AMI) defines two approaches to SerDes modeling and simulation flow: time domain or bit-by-bit simulation for nonlinear and/or time variant (NLTV) model and statistical simulation for linear and time invariant (LTI) model. Statistical simulation has advantages of faster simulation speed and arbitrary low BER floor under linear model assumption. However, majority high speed SerDes devices incorporation clock and data recovery (CDR) circuit and/or adaptation state machines which are not conducive to LTI modeling. This paper presents a unified SerDes modeling method for both simulation types. The results show close correlation between time and statistical simulations based on selected criteria. This paper demonstrates the feasibility of dual model approach to IBIS-AMI and summarizes simulation methods that are unique to each.

Authors Biography

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John Baprawski, consultant for Electronic System Level (ESL) Design. Since June 2010, he has focused on modeling high speed digital (HSD) integrated circuits (ICs) based on the industry Input/Output Buffer Information Specification (IBIS) Algorithmic Model Interface (AMI) standard. He created the Agilent Technologies AMI Training class based on their SystemVue and Advanced Design System (ADS) tools. He conducted AMI Training at over 30 high speed digital IC semiconductor companies and created many custom transmit (TX) and receive (RX) AMI models. Prior to this consulting work, John was the R&D manager at Agilent Technologies EEsof Division for 22 years with responsibility for initiating and evolving their system level design tools including OmniSys, ADS Ptolemy, Wireless Libraries and SystemVue products. He holds a Masters degree in Electrical Engineering from University of California, Los Angeles, and PhD studies at University of Michigan. His web site is www.johnbaprawski.com.

Cathy Ye Liu, the Distinguished Engineer, currently heads up LSI's SerDes Architecture group. Since 2002, she has been working on high speed SerDes solutions. Previously she has developed read channel and mobile digital TV receiver solutions. She received her B.S. degree in Electronic Engineering from Tsinghua University, China, in 1995 and received her M.S. and Ph.D. degrees in Electrical Engineering from University of Hawaii in 1997 and 1999, respectively. Her technical interests are signal processing and coding in high-speed SerDes.

1 Introduction

It is important and challenging to model high speed serial transceivers (SerDes) and to obtain behaviors that are closely matched to those from analog circuit simulations and silicon devices. Comprehensive modeling strategy and accurate simulation platform can serve many purposes such as performance prediction, architecture verification and implementation trade-off analysis. I/O Buffer Information Specification (IBIS) Version 5.0 [1] in August 2008 introduced algorithmic modeling interface (AMI) to meet with this need. Additional improvements are ratified in Version 5.1 [2] on August 24, 2012.

IBIS-AMI defines two approaches to SerDes modeling and simulation flow: time domain or bit-by-bit simulation for nonlinear and/or time variant (NLTV) model and statistical simulation for linear and time invariant (LTI) model. Statistical flow has advantages of faster simulation speed and arbitrary low BER floor given the LTI model assumption. However, majority high speed receivers [3-4] incorporate clock and data recovery (CDR) circuit and/or adaptation state machines which are not conducive to LTI modeling. Therefore, additional modeling and simulation considerations must be taken in order to make full usage of IBIS specifications and to meet with system designers' expectation on accuracy and speed.

This paper presents a unified SerDes modeling method for both simulation types. We focus on receiver (RX) model development and correlations. In Section 2, we first present an overview on IBIS-AMI model and simulation flow as contained in the latest IBIS specification. Section 3 follows with algorithmic modeling of 10+Gbs receiver in time domain. After bit accurate model behaviors are obtained, Section 4 discusses the process of prototyping a statistical model from its time domain kin based on selected state space mapping method. In Section 5, simulation methods of both flows are discussed and results from two types of receiver model are correlated. Summary of this work and enhancements for future modeling and simulation are provided in Section 6.

2 Overview of SerDes Model and Simulation Flow

2.1 IBIS-AMI

Figure 1 shows an example of simulation set up in EDA tools with IBIS-AMI SerDes models. With the AMI extension, IBIS specification intends to separate SerDes modeling and simulation into two parts: analog and algorithmic. The analog part of SerDes model may consist of termination which is assumed to be linear and time invariant. Termination model consists of resistors, capacitors and/or inductors to meet return loss requirements set forth by various industry standards such as IEEE. To fully capture insertion loss and reflections in simulation, in particular its frequency dependency behaviors, analog termination model will be best represented as a broadband S-parameter model [5]. EDA tools will concatenate IBIS analog model with external interconnect models and generate a combined channel impulse response.

The algorithmic part of SerDes model consists of mostly active circuit elements such as various equalizers, clock recovery and adaptation circuits. The implementation details of algorithmic model are provided in an executable library file. As such the algorithmic model is operating system (OS) dependent and it is important to match models with the requirements from the EDA software.

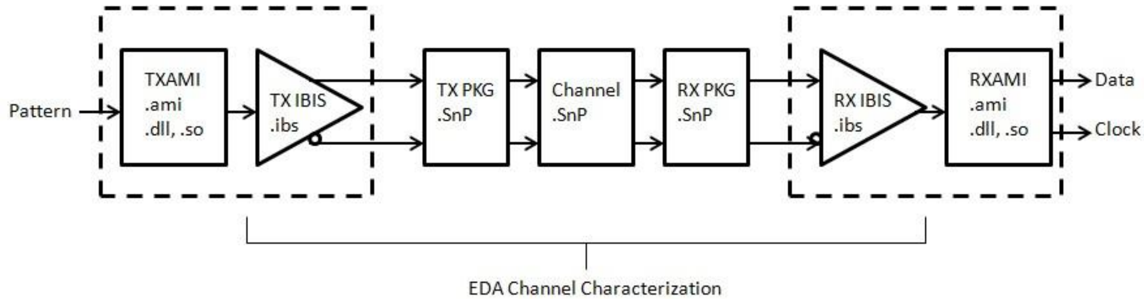

Figure 1 An example of IBIS-AMI model simulation set up in EDA tools

2.2 Algorithmic Model Development and Simulation Flow

IBIS-AMI further defines functions and interfaces supporting two types of algorithmic modeling and simulation flow: time domain and statistical domain. In time domain analyses, signal waveforms excited by given stimulus bit streams are calculated. SerDes equalizations and CDR are modeled by signal processing functions inside AMI_GetWave function, which closely tracks circuit implementation, adaptation algorithms and other nonlinear device behaviors. Physical channels are assumed to be LTI and their effects are treated with convolutions. The AMI time domain flow has shown good accuracy and simulation speed that is orders of magnitudes faster than SPICE based simulators.

Statistical flow is supported by the AMI_Init function and through exchanges of impulse responses between algorithmic model and EDA tools. The resulting impulses are used to calculate signal probability density functions (PDF) under the assumption that the entire link is LTI, including SerDes and physical channels. Utilizing powerful computational techniques [6-7], statistical calculations exhaust all possible bit patterns and are equivalent to running infinite number of bits, As a result, statistical flow is able to compute BER at arbitrarily low levels and achieves greater simulation performance than the time domain flow. Owing to the limitation of the LTI approximation, statistical simulations cannot account for nonlinearities such as adaptation and CDR.

In link analyses both time domain and statistical flows are desired. It is frequently necessary to model high speed SerDes in fine details [8]. A bit accurate model serves this purpose and can be often developed in the same partition as circuit implementation does. Additional modeling efforts will be required to enable a receiver statistical model that best approximate circuit dynamic behaviors for a given configuration and to make full use of EDA analysis methods. In the following sections, we investigate a rapid prototyping method for statistical model that is based on a bit accurate receiver model.

3 Time Domain Modeling Method for High Speed Receiver

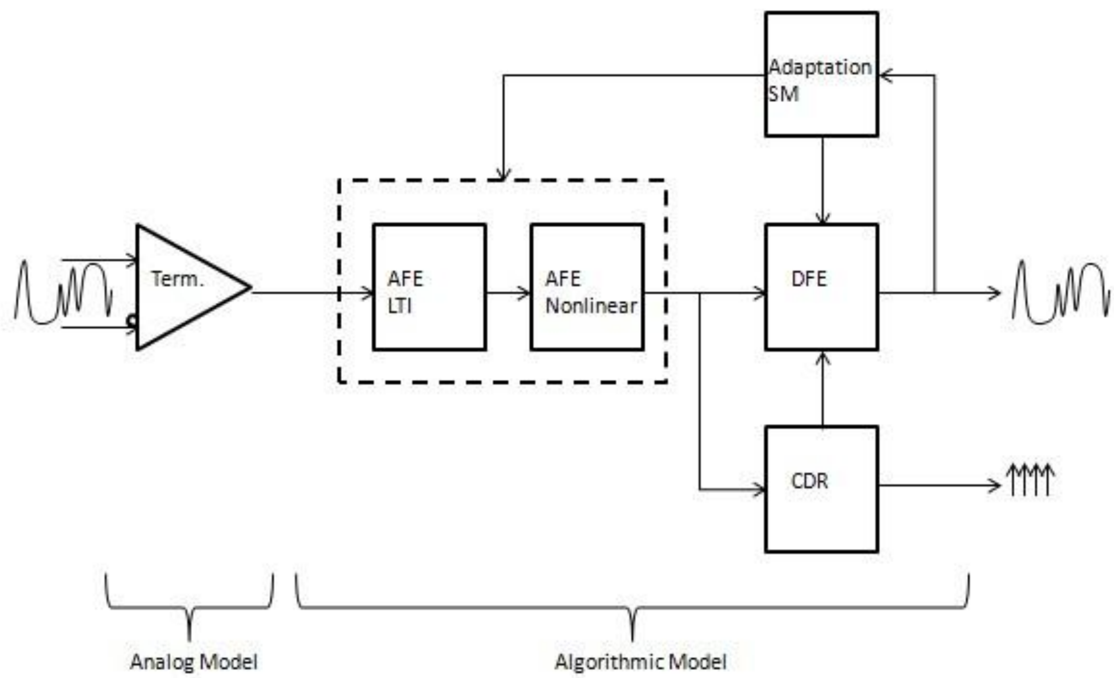

Figure 2 Block partition of an example receiver time domain model

3.1 Analog Front End

Analog front end (AFE) in general consists of cascading variable gain amplifier (VGA) block and continuous-time linear equalizer (CTLE) blocks. Controls on VGA gain and CTLE peaking (equalization) are often made automatically adaptive by use of an adaptation state machine. They can also be manually set through gain code and peaking code respectively. The manual controls are useful when charactering static model behaviors which can be subsequently used towards statistical model development. The modeling of VGA and CTLE are carried out using linear and/or nonlinear functions. Both functions are required to achieve closer correlations with circuit simulations. For receiver model under study in this paper, the linear function is further modified a non-linear one.

3.1.1 AFE Linear Model

The linear behavior of VGA and CTLE can be captured by measuring AC transfer functions of respective circuits. For closer correlations, AC transfer functions are extracted at various process voltage and temperature (PVT) corners, and for each control code values. Non-ideal signal buffers are often included in simulation for greater accuracy. These buffers often have limited bandwidth and non-unit gain/attenuation and may include multiplexer buffer and/or DFE summing buffer.

Once measured, AC transfer functions are fitted with poles and zeros in either continuous time domain (s-domain) or discrete time domain (z-domain). In s-domain modeling, convolution or Fourier transform is used to carry out filtering operation. But continuous time domain operation requires large sized buffers. To improve memory utilization and simulation speed, we can fit transfer functions with z-domain poles and zeros and deploy an infinite-impulse response (IIR) filter for filtering operation. However with z-domain filtering approach, discrete time filter coefficients require modifications with a change in the sampling frequency.

3.1.2 AFE Non-Linear Model

AC transfer functions are useful in capturing small-signal behaviors (linear behaviors) of the analog circuits. Large signal behaviors will require the use of non-linear functions such as hyperbolic tangent function or polynomial function. Here we consider the usage of a hyperbolic tangent function to implement AFE non-linear model.

Let $x(t)$ be the AFE input signal, $y(t)$ the linear filter output and input to the non-linear filter under development. The amplitude of $x(t)$ is chosen such that AFE circuit operates in non-linear mode. We can express $z(t)$ the AFE output from the non-linear model as:

$$z(t) = Asat * tanh(y(t)/Asat) \qquad \text{Equation 3-1.}$$

Where *Asat* is the non-linearity modeling parameter and has unit of volts.

The same signal $x(t)$ is applied to SPICE circuit simulation and output signal $w(t)$ is captured. The value of *Asat* is determined by minimizing the mean squared error (MSE) between filter output signal $z(t)$ and circuit output signal $w(t)$. Figure 3 shows eye diagram comparisons between the outputs of linear filter model (red), non-linear model (Blue) and SPICE (Green).

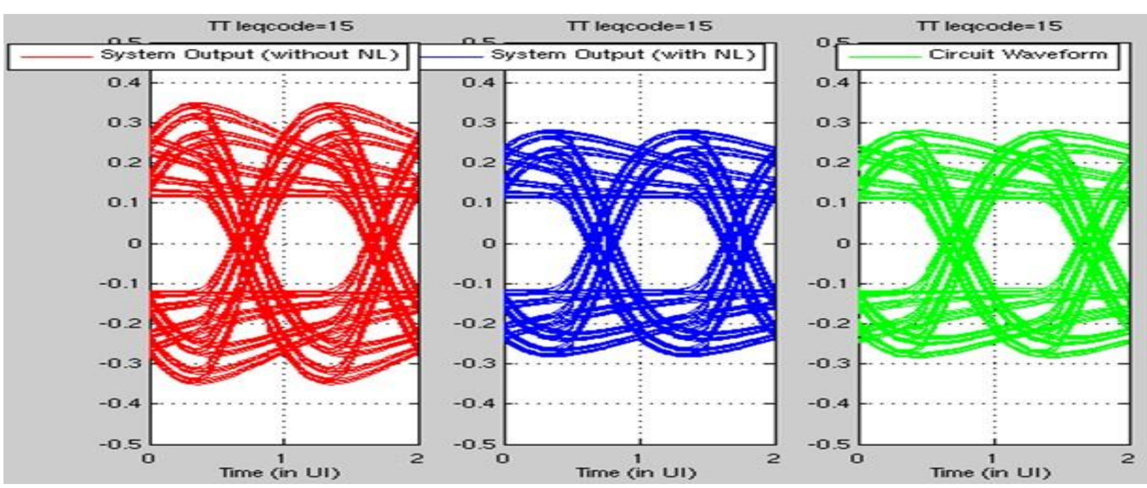

Figure 3 AFE correlations with SPICE circuit simulation results

3.2 Decision Feedback Equalizer

The decision feedback equalizers (DFE) can be modeled as a series of finite impulse response (FIR) filters. The DFE filter coefficients' range and resolution are obtained directly from analog circuit simulations at different PVT corners.

An exponential pulse shaping function is used to accurately model finite rise and fall time of DFE output signals. This pulse shaping function is designed to have matched outputs with the waveform from convolving the same bit sequence with the pulse response of DFE circuit. It is noted that rise and fall times are different at various PVT corners and shall be modeled as such.

3.3 Clock Data Recovery

CDR is a mathematic driven model. Two widely used CDR phase detectors include bang-bang phase detector (BBPD) and baud rate phase detector (BRPD). Here we consider the function of a BBPD.

Bang-bang phase detector behaves as a one-tap edge equalized DFE which minimizes the mean square error of the crossing sample. Its gradient is given as

$$e(k) * d(k-1) \qquad \text{Equation 3-2,}$$

where the error signal $e(k)$ is defined as:

$$e(k) = \begin{cases} x(k), & d(k) = -d(k-1) \\ 0, & d(k) = d(k-1) \end{cases} \qquad \text{Equation 3-3.}$$

Here $x(k)$ is the crossing sample between data samples $d(k-1)$ and $d(k)$. To alleviate the situation where the phase is stuck at the signal crossing, the gradient is forced to be 1 or -1 if $x(k) = -d(k) = -d(k-1)$.

3.4 Adaptation State Machine

Complex receiver often has many adaptation loops that aim to place receiver in optimal operating states given an incoming signal. The received signals embody channel effects, transmitter settings and other impairments such as jitter and noise. For the receiver under study, CDR phase, DFE tap coefficients, VGA gain and CTLE peaking are implemented as several interacting loops and are placed under control from the adaptation state machine.

Receiver adaptation loops consist of one or more stages of digital accumulators, which are used to obtain time average of the respective adaptation gradient. Often delay elements are deployed in the signal path. The digital accumulators and the amount of delay can be modeled in fixed point algorithms to enable direct correlation between IBIS-AMI model behaviors and circuit behaviors from SPICE or AMS simulations. With this approach, faster IBIS-AMI model simulations can be used to thoroughly investigate the impact of delay elements at each adaptation stages.

4 Prototyping Method for a Receiver Statistical Model

4.1 State Space Definition

It is not feasible to capture dynamic behaviors of a bit accurate model in statistical domain. However, it is possible to approximate a bit accurate model at one instant where behaviors may be considered static. We call this instant a state or an operating condition and a collection of states a state space. Our goal is to prototype a statistical receiver model whose behaviors closely match to those of the bit accurate model across the entire state space [9-10].

The states of a bit accurate receiver model are influenced by many external and internal factors. External factors may include transmitter settings (amplitude and pre-emphasis), interconnect selections (channel and package), bit patterns and bit rates. Internal factors may include adaptation algorithm (dithering), convergence rate and run length of time domain simulation. A time domain model will have infinite possible states. It is important to clearly define a reasonable sized state space more representative of actual system settings. An example state space is shown in Table 1. Typical state space will have 30 or more entries.

Table 1 An example state space for 12Gbs bit rate

State	**Pattern**	**Run length**	**Transmitter**		**Interconnect**	
			Amplitude	PreEmphasis	Package	Channel
1	TP2	1M UI	1200 mV	P7	TC	10 m
2	Scramble0	1M UI	1000 mV	P0	TC	60 cm
3	PRBS 11	1M UI	1200 mV	P4	TC	100 m
4	PRBS 11	1M UI	1000 mV	P4	TC	60 cm
5	PRBS 11	1M UI	800 mV	P4	TC	60 cm
6	PRBS 11	1M UI	400 mV	P4	TC	60 cm

4.2 Statistical Model Partition

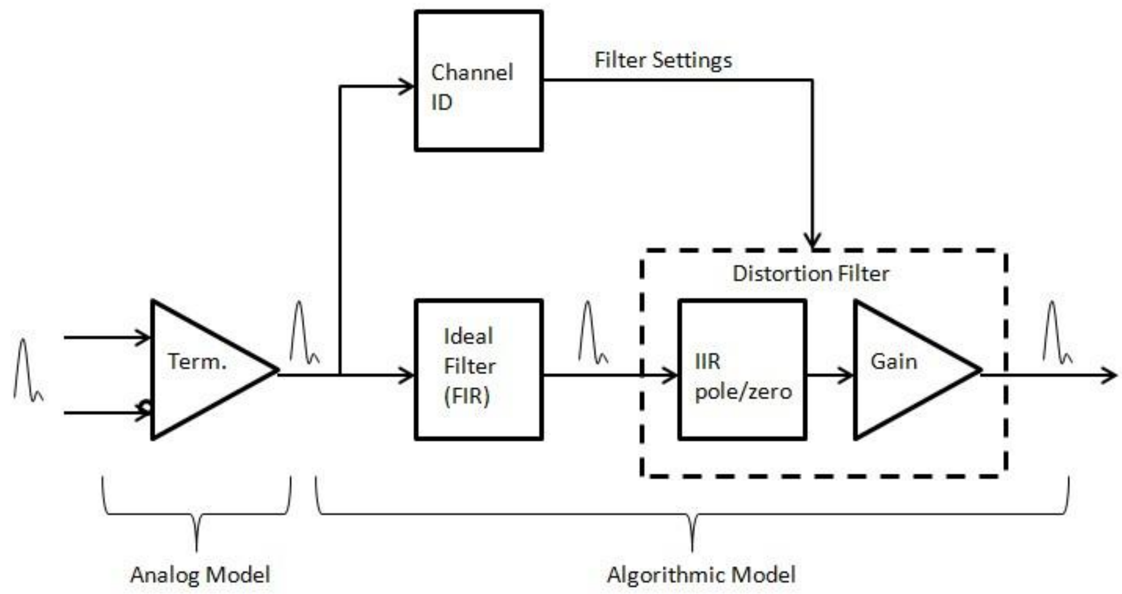

Figure 4 Prototype of statistical model

Statistical model is partitioned into two parts: a channel identification block and a LTI equalizer. The LTI equalizer consists of two signal processing stages that are serially connected. As the statistical model is LTI in nature, the order of these two stages is not significant. In Figure 4, the first stage provides ideal filtering while the second stage introduces distortions so that model behaviors will be able to match to those obtained from a bit accurate model.

Ideal filter can include receiver LTI equalizers such as aforementioned linear functions from VGA and CTLE. However, simple FIR filters are often sufficient for statistical model prototype. Ideal filter coefficients are derived from impulse response characterization of receiver input by the EDA tool. Impulse response will include effects from transmitter LTI equalizer, transmitter die model, transmitter package model, system interconnect model, receiver package model and receiver die model.

Implementation of distortion filters can vary and may include IIR filters with tunable poles and/or zeros, gain and additional feed forward equalizers (FFE) if desirable. Settings for these signal processing units are tabled for each entry in the state space inside the model. Therefore at these defined states, good correlation results are achievable based on selected criteria. We will discuss correlation criteria in the next section along with simulation results.

The function of channel identification block is to determine which set of distortion filters to use. Impulse response at receiver input is provided by EDA software from a SPICE simulation. From impulse response, we can sort incoming signals based on frequency responses at defined frequency bands. When a given impulse response is identified between two pre-characterized states, linear interpolation is applied to obtain a set of suitable distortion filter controls.

5 Receiver Correlation in Time Domain and Statistical Domain Simulations

5.1 Simulation Methods

5.1.1 Analog Channel Impulse Response Characterization

In AMI simulations analog channels are assumed to be linear and represented by impulse responses. Channels may consist of link models, packages and terminations that come with IBIS models. Impulses responses from victim and aggressor TXs to RXs are characterized by SPICE simulations [5] to generate a comprehensive impulse matrix that is utilized by SerDes models. In physical channels, signal transmitted from a TX can be reflected multiple times at any port, resulting in multiple propagation paths between a pair of TX and RX. Multiple reflections are automatically included in every impulse by solving KCL boundary conditions at all ports. Thus, when S-parameters are used to represent a channel with crosstalk, a full multi-port S-parameter matrix, as illustrated in Figure 5, is recommended to account for every possible signal path that connects victims and aggressors.

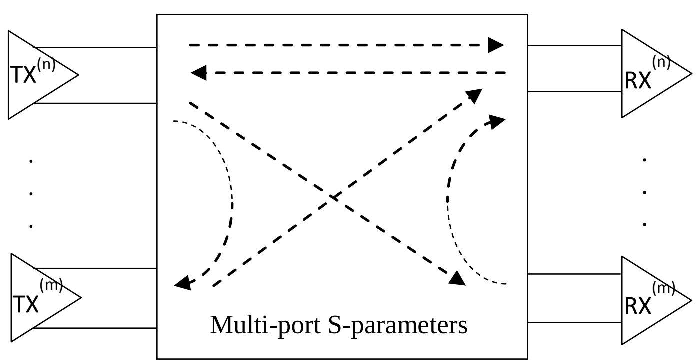

Figure 5 S-parameters representation of analog channel with crosstalk.

5.1.2 Time Domain Simulation

In this example, TX model does not implement the AMI_GetWave function, while RX model does. The time domain simulation flow is shown in Figure 6.

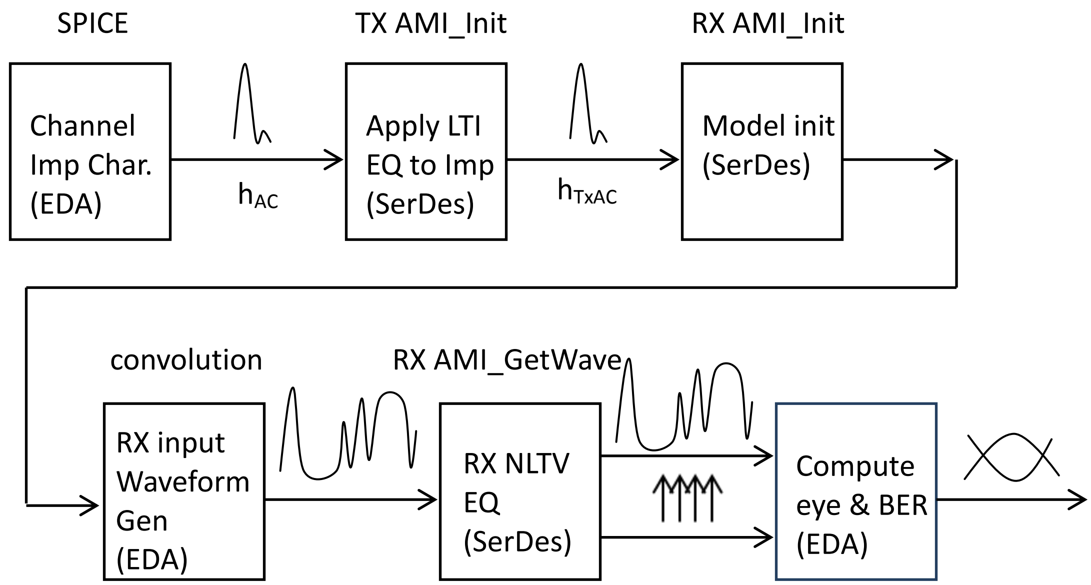

Figure 6 Time domain simulation flow. h_{AC} denotes the analog channel impulse responses and h_{TxAC} the modified impulse returned by TX AMI_Init.

After channel characterizations and AMI_Init calls, the differential signal at the RX input, v_{RxIn}, is calculated by the summation of signals transmitted by all TXs as shown in Figure 7.

$$v_{RxIn} = \sum_n h_{TxAC}^{(n)} * b^{(n)} \qquad \text{Equation 5-1}$$

where $b^{(n)}$ is the square waveform that represents the n^{th} TX's stimulus bit stream and $h_{TxAC}^{(n)}$ the impulse response from this TX to the RX that is returned by the TX AMI_Init function and a combined impulse of the TX equalizer (EQ) and the analog channel. Waveform v_{RxIn} is then input to RX AMI_GetWave, whose output waveform is used to calculate the eye and BER. Note that $b^{(n)}$ can have different patterns and data rates in different TXs. Asynchronous crosstalk can be simulated by using a small offsets in data rates between aggressor and the victim channels.

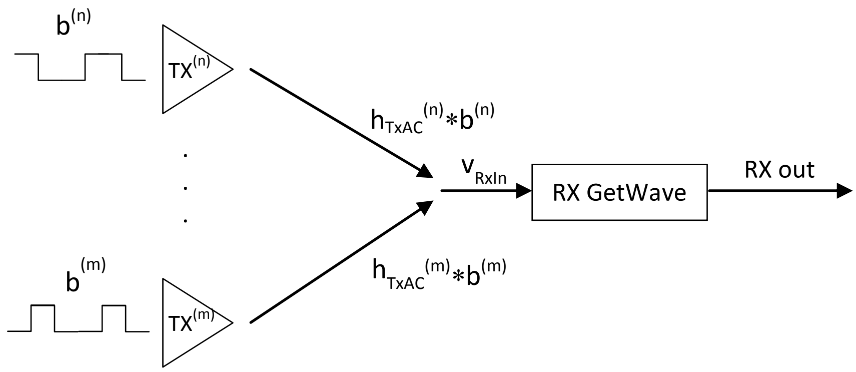

Figure 7 RX input signal calculations.

TX jitters are applied to transitions in the TX input square waveform $b^{(n)}$ as shown in Figure 8. Rise and fall edge positions are modulated by jitters as

$$
\begin{aligned}
t_r(i) &= n_r(i)\cdot T + \tau_r(i) \\
t_f(i) &= n_f(i)\cdot T + \tau_f(i)
\end{aligned}
\qquad \text{Equation 5-2}
$$

where $t_r(i)$ and $t_f(i)$ are rise and fall times of the i^{th} pulse in $b^{(n)}$, $n_r(i)$ the bit index of the first 1-bit of the pulse and $n_f(i)$ the index of the first 0-bit that follows the pulse. T is the unit interval. Terms $n_r(i)T$ and $n_f(i)T$ represent ideal rise and fall times, and $\tau_r(i)$ and $\tau_f(i)$ are jitters.

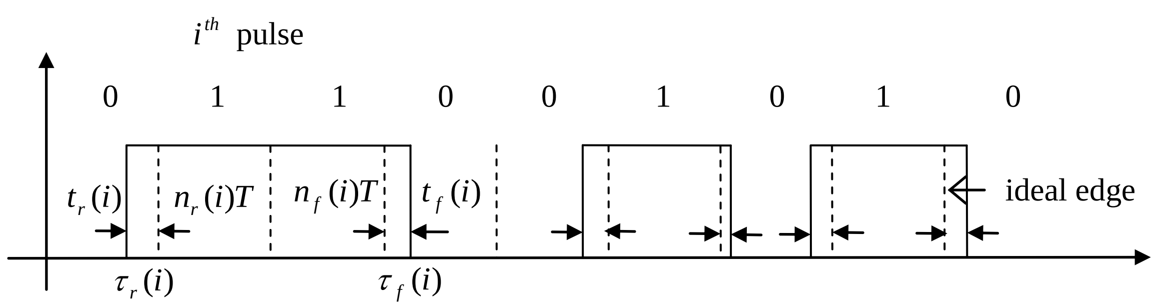

Figure 8 TX jitter model. Solid vertical lines represent the actual rising and falling edges. Dash lines represent ideal edges.

Various jitter components defined in the IBIS-AMI standard, including clock duty-cycle-distortion (DCD), deterministic jitter (DJ), sinusoidal jitter (SJ) and random jitter (RJ), are considered. In terms of DJ, RJ, PJ and DCD contributions,

$$
\begin{aligned}
\tau_r(i) &= \eta_r^{DJ}(i) + \eta_r^{RJ}(i) + A\cos[\omega\cdot n_r(i)T + \phi] + (-1)^{n_r(i)}\frac{\Delta}{2} \\
\tau_f(i) &= \eta_f^{DJ}(i) + \eta_f^{RJ}(i) + A\cos[\omega\cdot n_f(i)T + \phi] + (-1)^{n_f(i)}\frac{\Delta}{2}
\end{aligned}
\qquad \text{Equation 5-3}
$$

where η_r^{DJ} and η_f^{DJ} represent DJ at the rise and fall edges; η_r^{RJ} and η_f^{RJ} represent RJ that is typically described by a Gaussian distribution; A and ω are SJ amplitude and frequency; and Δ terms model clock DCD. Waveform $b^{(n)}$ can be written in terms of $t_r(i)$ and $t_f(i)$ as

$$b^{(n)}(t) = \sum_i \left[\Theta(t - t_r(i)) - \Theta(t - t_f(i))\right] - \frac{1}{2} \qquad \text{Equation 5-4}$$

where Θ is the unit step function. It is worth pointing out that by convolving $b^{(n)}$ with the channel impulse response TX jitter is amplified by the channel loss, a phenomenon that has been confirmed by measurements, simulations and theory [7, 11].

In time-domain simulations, CDR jitter is captured in clock times generated by the RX AMI_GetWave function, which are used to center waveform sampling when constructing eye diagrams. As a result, CDR jitter impairment is included in eye and BER calculations. Time-domain analysis typically runs several million bits due to simulation speed limitations. A BER extrapolation or fitting method will be used to predict eye margins at 10^{-12} BER or below.

5.1.3 Statistical Simulation

The statistical simulation flow is shown in Figure 9. The impulse returned by RX AMI_Init captures effects of the TX EQ, the analog channel and the RX EQ and is a combined representation of the entire link. It is used to compute eye probabilities in statistical simulations. With an impulse length of M bits, the number of bit patterns relevant to the channel output at a given time t and logic level is 2^{M-1}. According to Eq. 5-4, for the m^{th} pattern, the channel output $v^{(m)}(t)$ is

$$v^{(m)}(t) = \sum_i h_{TxACRx} * \left[\Theta(t' - t_r^{(m)}(i)) - \Theta(t' - t_f^{(m)}(i)) - \frac{1}{2}\right] \qquad \text{Equation 5-5}$$

where $t_r^{(m)}(i)$ and $t_f^{(m)}(i)$ are rise and fall times of the i^{th} pulse in the m^{th} pattern and h_{TxACRx} the impulse returned by RX AMI_Init. The output PDF of a given logic level is

$$p(v,t) =$$
$$\frac{1}{2\pi}\int_0^{2\pi} d\phi \frac{1}{2^{M-1}} \sum_m \int \delta[v - v^{(m)}(t)] \cdot \prod_i \left\{ \begin{array}{l} g[\eta_r^{(m)}(i)^{RJ}] \cdot g[\eta_f^{(m)}(i)^{RJ}] \\ \cdot\, d[\eta_r^{(m)}(i)^{DJ}] \cdot d[\eta_f^{(m)}(i)^{DJ}] \end{array} \right\} \qquad \text{Equation 5-6}$$
$$\cdot\, d\eta_r^{(m)}(i)^{RJ} \cdot d\eta_f^{(m)}(i)^{RJ} \cdot d\eta_r^{(m)}(i)^{DJ} \cdot d\eta_f^{(m)}(i)^{DJ}$$

where $\eta_r^{(m)}(i)^{RJ}$, $\eta_f^{(m)}(i)^{RJ}$, $\eta_r^{(m)}(i)^{DJ}$ and $\eta_f^{(m)}(i)^{DJ}$ are RJ and DJ at rising and falling edges of the i^{th} pulse in the m^{th} pattern, $g(\eta)$ the RJ PDF, and $d(\eta)$ the DJ PDF [11].

The same TX jitter model used in time domain simulations is described by Eqs. 5-2 and 5-3 is employed in statistical simulations. Jitters are embedded in rise and fall times $t_r^{(m)}(i)$ and $t_f^{(m)}(i)$ of the stimulus, providing consistent treatment of TX jitter between time domain and statistical flows. As indicated by Eq. 5-5, jitter amplification by the channel is also taken into account in statistical calculations.

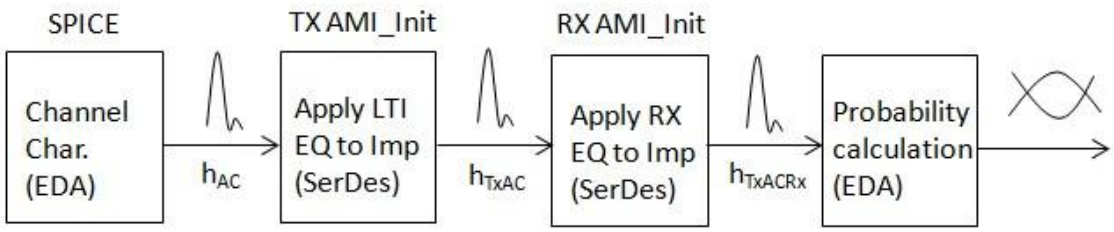

Figure 9 Statistical simulation flow. h_{AC} denotes the analog channel impulse responses, h_{TxAC} the modified impulse returned by TX AMI_Init, and h_{TxACRx} the modified impulse returned by RX AMI_Init

Figure 8 shows that TX jitters, including the RJ component, are intrinsically pattern dependent because they only occur at transitions. The summation of pattern index m in Eq. 5-6 is the consequence of this dependency, which introduces tremendous computation complexity to statistical simulations. A highly efficient linear programming technique is applied to cope with this complexity [11], ensuring fast and rigorous evaluation of Eq. 5-6 without any approximation, such as small jitter linearization or low probability extrapolation. The algorithm is extended to include the 8B10B coding constraints on bit patterns.

RX jitters are applied to statistical results in post-processing by convolving p(v,t) with jitter PDFs. Crosstalk effects are taken into account by combining PDFs of the main channel signal and crosstalk noise. For synchronous crosstalk,

$$p(v,t) = \int p_{main}(v - v_1 - v_2 \cdots - v_n, t)\, p_{xtlk}^{(1)}(v_1,t)\, p_{xtlk}^{(2)}(v_2,t) \cdots p_{xtlk}^{(n)}(v_n,t)\, dv_1 dv_2 \cdots dv_n \qquad \text{Equation 5-7}$$

where p_{main} and $p_{xtlk}^{(i)}$ are the PDFs of the main channel and the i^{th} crosstalk aggressor calculated by Eq. 5-6. For asynchronous crosstalk,

$$\begin{aligned} \overline{p}_{xtlk}^{(i)}(v) &= \frac{1}{T^{(i)}} \int p_{xtlk}^{(i)}(v,t)\,dt \\ p(v,t) &= \int p_{main}(v - v_1 - v_2 \cdots - v_n, t)\, \overline{p}_{xtlk}^{(1)}(v_1)\, \overline{p}_{xtlk}^{(2)}(v_2) \cdots \overline{p}_{xtlk}^{(n)}(v_n)\, dv_1 dv_2 \cdots dv_n \end{aligned} \qquad \text{Equation 5-8}$$

where $T^{(i)}$ is the unit interval of the i^{th} crosstalk channel.

5.2 Correlation Criteria Selection

Signal waveform has multiple characteristics: rise time, fall time, high level, low level, just to name a few. For serial link analysis, continuous-time signal waveforms are often mapped to eye diagram which yields additional eye metric parameters such as eye width, eye height (inner and outer), crossing width, etc. Clearly no single criteria can completely define output waveforms from a receiver time domain model. During statistical model prototyping, iterations are required to achieve convergence of control values when multiple correlation criteria are selected.

In the following simulations, we show two sets of correlation criteria in Table 2 and Table 3 and discuss the performance of resulting statistical model.

Table 2 Correlation criteria based on SNR and level-1

Distortion Filter	**Correlation Criteria**	**Criteria Function**
IIR	Signal-to-Noise Ratio (SNR)	Measure the ratio of eye amplitude and the sum of standard deviations of the logic-1 and logic-0 histograms.
Gain	Level 1	Measure mean value of logic-1 level across the eye level boundary.

Table 3 Correlation criteria based on rise time and level-1

Distortion Filter	**Correlation Criteria**	**Criteria Function**
IIR	Rise Time	The average time from low to high amplitude thresholds.
Gain	Level 1	Measure mean value of logic-1 level across the eye level boundary.

5.3 Correlation Results of Receiver Models

5.3.1 Correlation at 12Gbs with SNR and Level-1

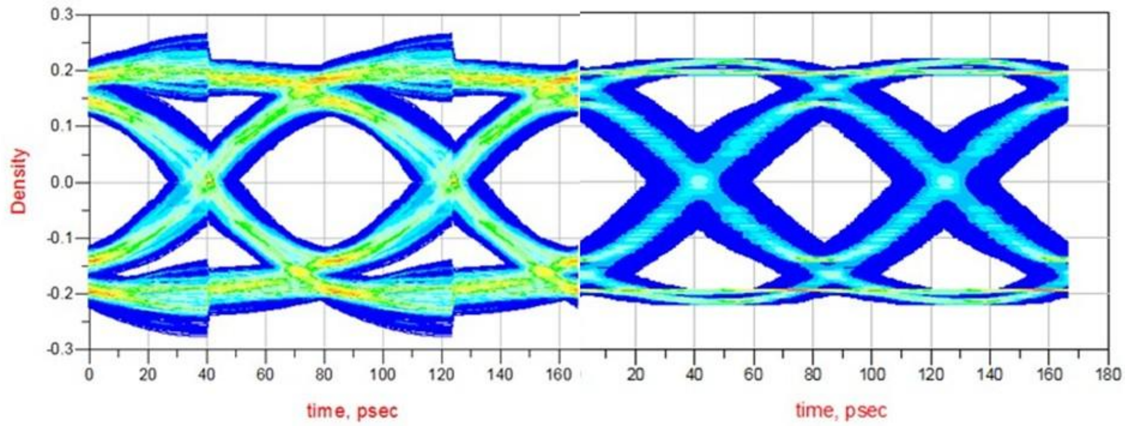

Figure 10 12Gbs eye comparison between time domain (left) and statistical domain (right)

Table 4 Comparison of signal characteristics at 12Gbs

Measurement	Time Domain	Statistical
Level 1	165 mV	165 mV
Level 0	-165 mV	-165 mV
Amplitude	330 mV	330 mV
Height	199 mV	185 mV
Width	59.58 ps	59.83 ps
SNR	6.878	6.879
Rise Time	38.47 ps	41.28 ps
Fall Time	38.50 ps	42.02 ps
Jitter (RMS)	4.000 ps	3.923 ps

5.3.2 Correlation at 6Gbs with SNR and Level-1

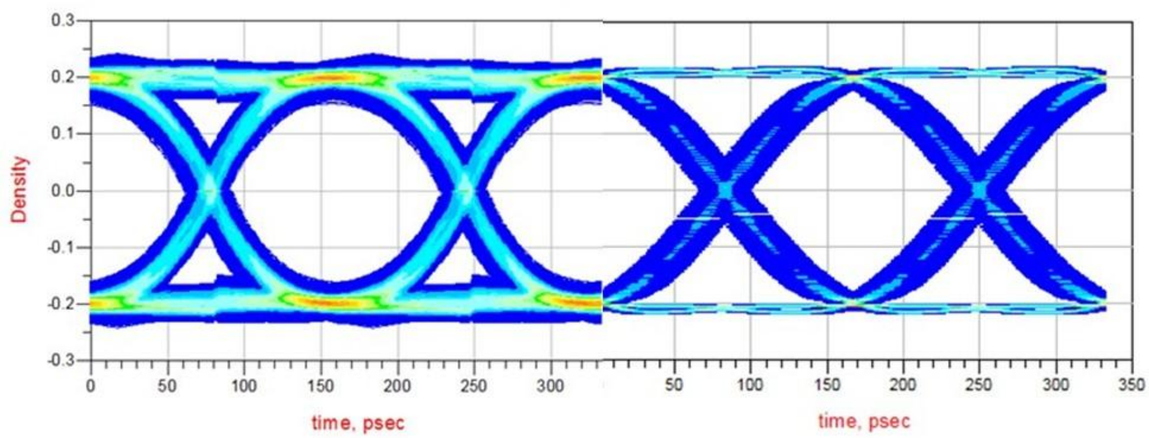

Figure 11 6Gbs eye comparison between time domain (left) and statistical domain (right)

Table 5 Comparison of signal characteristics at 6Gbs

Measurement	Time Domain	Statistical
Level 1	198 mV	197 mV
Level 0	-198 mV	-198 mV
Amplitude	397 mV	395 mV
Height	344 mV	343 mV
Width	140.8 ps	144.7 ps
SNR	22.839	22.814
Rise Time	53.00 ps	74.44 ps
Fall Time	52.99 ps	73.33 ps
Jitter (RMS)	4.326 ps	3.652 ps

5.3.3 Correlation at 3Gbs with Rise Time and Level-1

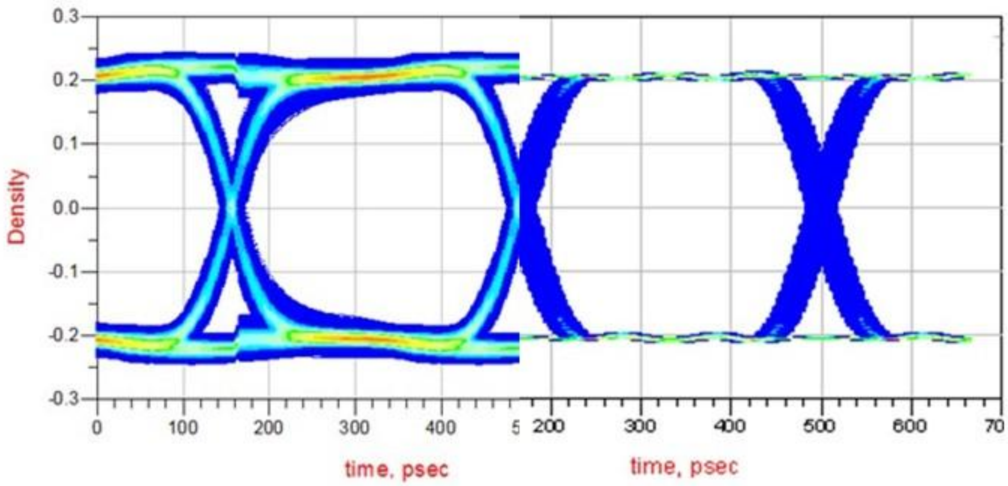

Figure 12 3Gbs eye comparison between time domain (left) and statistical domain (right)

Table 6 Comparison of signal characteristics at 3Gbs

Measurement	Time Domain	Statistical
Level 1	206 mV	207 mV
Level 0	-206 mV	-207 mV
Amplitude	412 mV	414 mV
Height	373 mV	402 mV
Width	311.8 ps	311.7 ps
SNR	31.980	100.575
Rise Time	53.51 ps	53.33 ps
Fall Time	53.55 ps	53.33 ps
Jitter (RMS)	3.617 ps	3.757 ps

5.3.4 Correlation at 1.5Gbs with Rise Time and Level-1

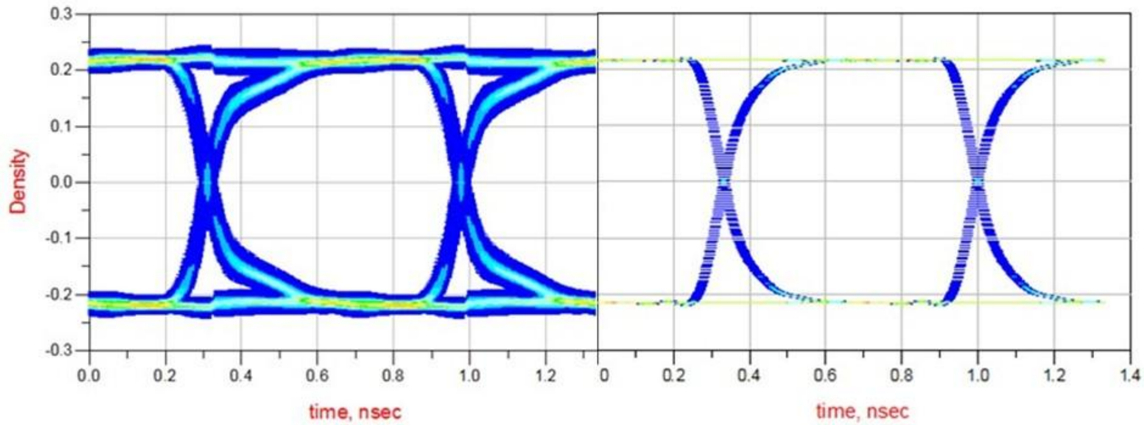

Figure 13 1.5Gbs eye comparison between time domain (left) and statistical domain (right)

Table 7 Comparison of signal characteristics at 1.5Gbs

Measurement	Time Domain	Statistical
Level 1	215 mV	215 mV
Level 0	-215 mV	-215 mV
Amplitude	429 mV	430 mV
Height	397 mV	426 mV
Width	626.7 ps	642.6 ps
SNR	39.717	100.525
Rise Time	93.23 ps	93.33 ps
Fall Time	93.94 ps	93.33 ps
Jitter (RMS)	7.051 ps	3.535 ps

6 Conclusions and Future Work

In this paper, a unified SerDes modeling method is presented for IBIS-AMI applications. Detailed algorithmic modeling of 10+Gbs receiver is first developed for time domain simulation flow. We show that rapid prototyping a statistical model can be achieved on an NLTV model based on selected state space mapping method. Good correlations are obtained between both types of receiver model using selected criteria.

Future work include enhancing statistical model with additional correlation criteria, improving model behaviors at interpolated states and at states out of bound, and correlating crosstalk behaviors of both model types.

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