Channel Simulation using SerDesDesign.com 2020/02/13

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About SerDesDesign.com

- Focused on Cloud based behavioral modeling and simulation of multi-gigabit high speed digital (HSD) integrated circuits (ICs) used in serializer/deserializer (SerDes) channels/systems.
- Features: Details at IntroductionToSerDesDesign.com
  - Free and subscription-use of on-line tools.
  - Tools for creating custom SerDes system IBIS-AMI models and SystemVue models.
    - IBIS-AMI models are portable for use in any standards compliant SerDes system channel simulator.
  - Consulting and training for custom IBIS-AMI modeling.
- SerDesDesign.com provides quick, efficient, accurate and cost effective modeling for SerDes systems.

About SerDesDesign.com

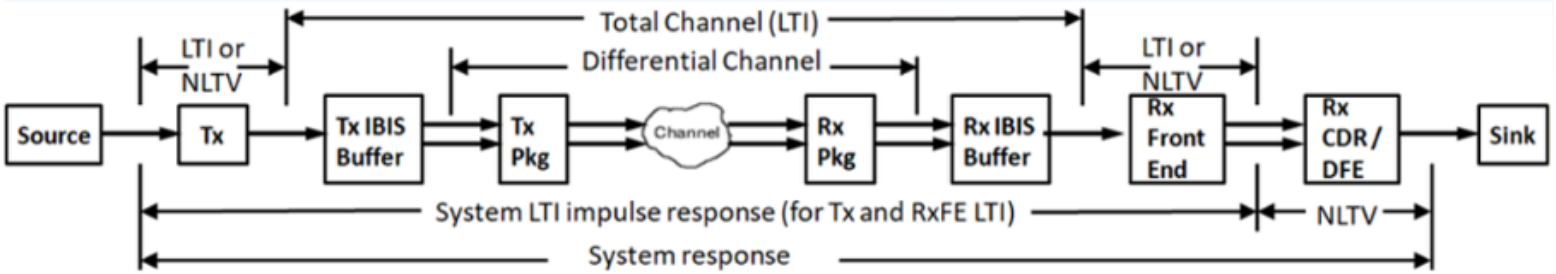
- All SerDesDesign.com simulation and modeling technology is based on Intellectual Property (IP) created by John Baprawski for John Baprawski Inc (DBA SerDesDesign.com).
- This IP was independently created by John Baprawski and does not use any third party protected IP.
- All SerDesDesign.com simulation and modeling technology is based on custom SystemVue models.
- SystemVue is the superior model development environment available from Keysight Technologies Inc.

What this training is and is not:

- First what this training is not:
  - Not focused on understanding SerDes systems in general.
  - Not for understanding details in SerDes system modeling.
  - Not an introduction to Channel Simulation or the IBIS-AMI standard.
  - Not an introduction to SerDesDesign.com
- What this training is:
  - The training is focused on learning about built-in functionality used in the SerDesDesign.com Channel Simulator.
  - The objective is to give SerDesDesign.com users an overview on the built-in Transmit (Tx) models, channel models and Receive (Rx) models and their use in the SerDesDesign.com Channel Simulator.

Typical SerDes System Block Diagram

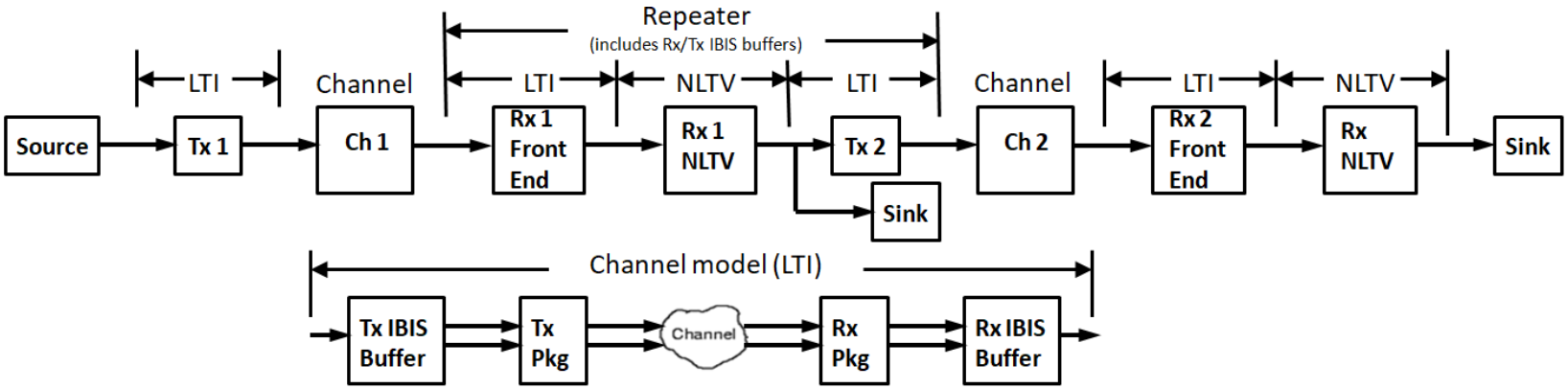
- **<u>Single Channel SerDes System</u>**



- Source: NRZ or PAM4 data source
- Tx: Transmiter equalization; typically an FFE; see **<u>Note</u>** below.
- Tx/Rx IBIS Buffers: IBIS buffer to the differential channel; defines the on-die impedance; see **<u>Note</u>** below.
- Tx/Rx Pkg: Package characteristic defined in a S4P file.
- Channel: SerDes channel defined in a S4P file.
- Rx Front End: Receiver equalization; typically a CTLE; see **<u>Note</u>** below.
- Rx CDR/DFE: Receiver timing/eq; typically a CDR and DFE; see **<u>Note</u>** below.
- **<u>Note</u>**: Can be a built-in model or a user defined IBIS-AMI model.

Typical SerDes System Block Diagram

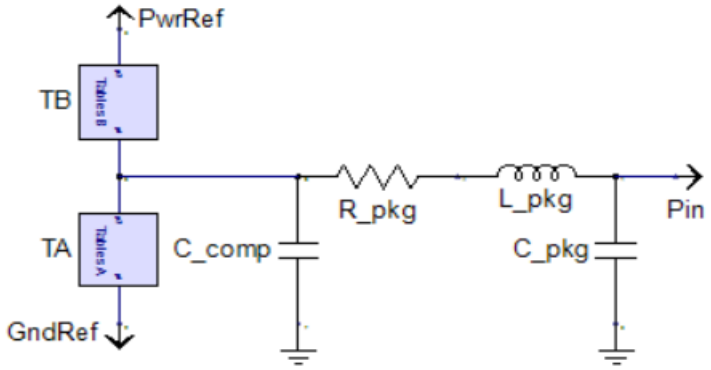
- **Single Repeater SerDes System**



- Source/Tx/Rx/IBIS Buffers/Pkg/Channel are as defined in the prior slide.
- The Repeater cascaseds two single channel systems.
- The Rx1 Front End (including Rx IBIS buffer), Rx1 NLTV and Tx2 (including Tx IBIS buffer) are combined to form the Repeater.
- The Repeater can be a Redriver (no symbol regeneration before Tx2) or a Retimer (with symbol regeneration before Tx2).

Typical Channel Models

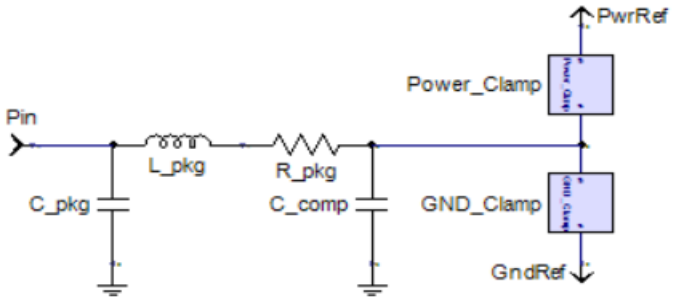
- The Tx IBIS Buffer is defined per the IBIS standard as a circuit or S-parameter file for corner cases: Typical, Min, Max.
- The Tx IBIS buffer circuit per output pin has this form:



  - The IBIS buffer can be selected from one listed in an IBIS [Model Selector].
  - The user can specify C/L/C_pkg, C_comp, and Tables A/B.
  - Tables A/B represent [Pullup]/[Pulldown] IV tables, [Ramp] table, and optionally [Rising Waveform]/[Falling Waveform] VT tables.
- In place of this circuit, the Tx IBIS buffer can be represented with S-parameter files per the IBIS 7.0 standard.

Typical Channel Models

- The Tx Package, Channel and Rx Package can be defined using S-Parameter files; SNP where N >= 4.
- The Rx IBIS Buffer is defined per the IBIS standard as a circuit or S-parameter file for corner cases: Typical, Min, Max.
- The Rx IBIS buffer circuit has this form:



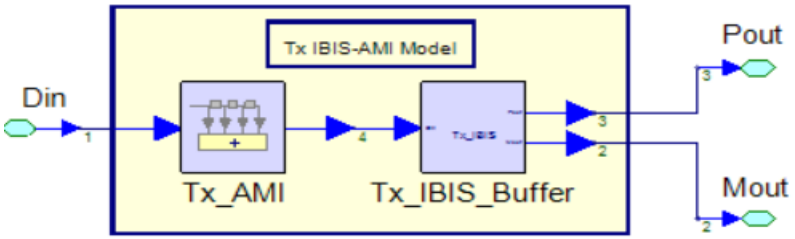
  - The IBIS buffer can be selected from one listed in an IBIS [Model Selector].
  - The user can specify C/L/C_pkg, C_comp, and IV Tables [GND_Clamp]/[Power_Clamp].
- In place of this circuit, the Rx IBIS buffer can be represented with S-parameter files per the IBIS 7.0 standard.

Typical Channel Models

- Example for the analysis of a typical channel.
  - SerDesDesign_Example_Channel_Model.pdf
  - Example includes Tx IBIS buffer, Tx Pkg S4P, channel S4P, Rx Pkg S4P, Rx IBIS Buffer.
  - Uses SerDesDesign.com channel-analysis-tool
  - The resultant single ended impulse response (h21dd) representing the differential channel can be downloaded and used in the SerDesDesign.com Channel Simulator or other Channel Simulators.

Typical Tx Models

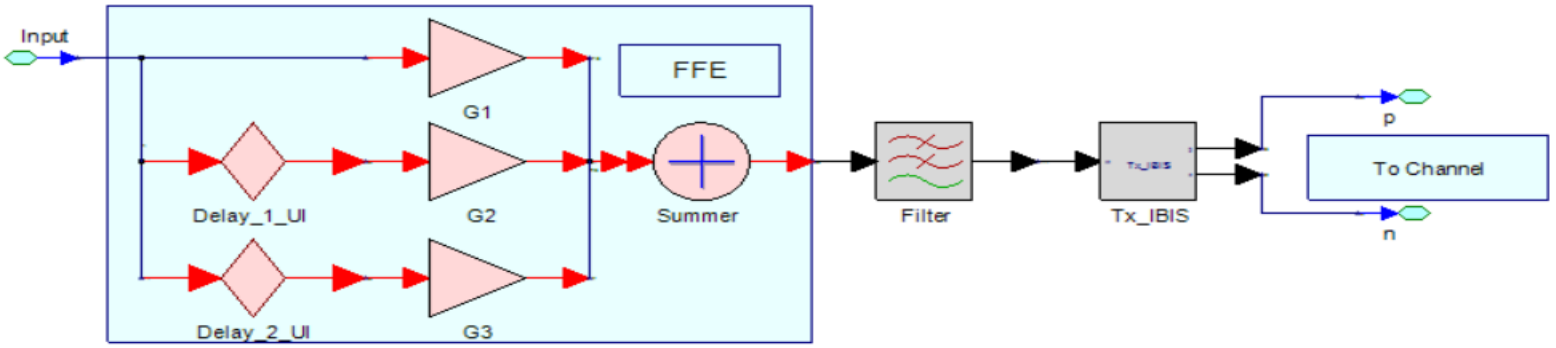
- The SerDes system Tx circuit is modeled as a Tx IBIS-AMI model per the IBIS-AMI standard with an AMI portion and an IBIS portion as shown here.



- The Tx IBIS Buffer characteristic is included into the total single ended impulse response between the Tx_AMI and Rx_AMI models.
- Conceptually, the Tx_AMI portion takes an input single ended NRZ (or PAM4) data stream and outputs a filtered NRZ single ended data stream. The Tx IBIS Buffer receives that single ended signal and outputs a differential signal that is connected to a differential channel.
  - For the Channel Simulator Statistical mode, the Tx LTI model converts its input impulse response to an output impulse response.
- This Tx IBIS-AMI model is typically defined as linear and time invariant (LTI) or as as nonlinear and/or time variant (NLTV).

Typical Tx Models

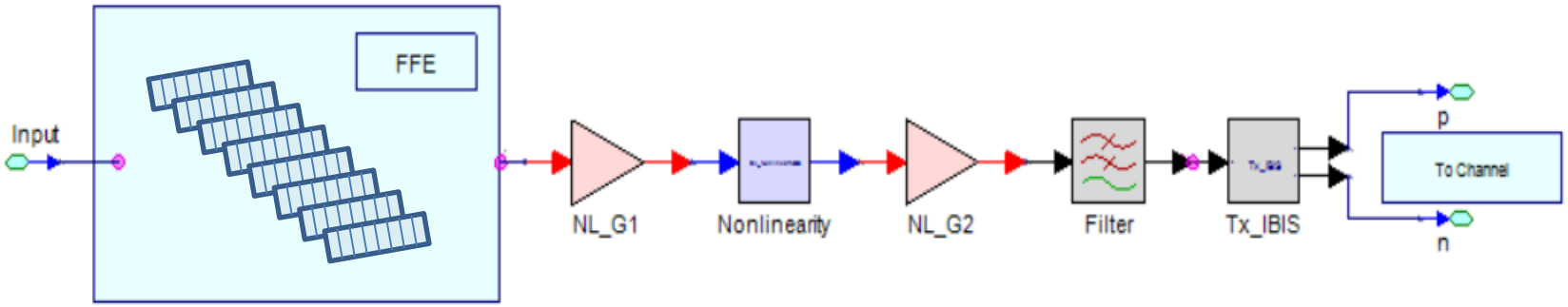
- The are many options for modeling a SerDes Tx circuit; a few are highlighted here.
  - All Tx models can have input source jitter defined (Rj, Dj, DCD, Sj/SjFreq).
- Tx circuit modeled as an FFE (feed-forward equalizer) using tap codes.



  - This figure shows 1 precursor (G1) and one post cursor (G3), but any number of pre and post cursors are allowed.
  - The taps are defined at quantized levels from a min to max value with defined step size.
  - The taps are specified with integer codes.
  - The filter can be specified for corners (Typical, Slow, Fast).
  - The tap codes can be automatically optimized for the given total channel.

Typical Tx Models

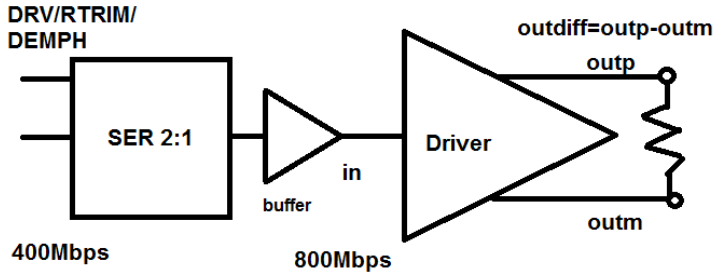
- Tx circuit modeled as an FFE (feed-forward equalizer) using bit registers.



  - 8 eight bit registers are used to define the FFE pecursor, main cursor and post cursor.
  - The number of active registers can be specified (1 to 8).
  - Each bit represents a voltage level; each bit can be assigned to a cursor with defined polarity (+ or -).
  - The Tx filtering response is captured for each set of registers (1 to 8) with all bits assigned to the main tap.
  - The Tx nonlinearity is derived from this Tx response.
  - The Tx filtering characteristic is interpolated from these responses based on the actual Tx FFE tap settings used.
  - The register bit settings can be automatically optimized for the given total channel.

Typical Tx Models

- The Tx circuit can be modeled as a black box for a 2 or 3 tap FFE.
- The Tx circuit is defined as shown in this figure.



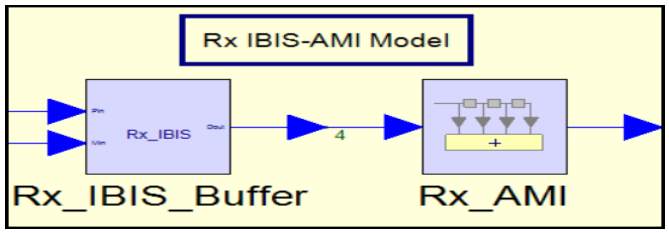
- The bit rate can range from a min to max value.
- The points from ‘in’ to ‘outdiff=outp-outm’ are modelled as a block box by collecting waveforms with a defined load Rload.
- The driver data can be defined for three corner cases: Typical, Slow, Fast.
- FFE gains (G1, G2, G3) and filters (F1, F2, F3) are derived from the data.
- The IBIS portion can be de-embedded to obtain the AMI portion.
- The Tx data can be optimally selected for the given total channel.

Typical Tx Models

- Example for a Tx circuit black box model.
  - Documentation: SerDesDesign_Example_Tx_Circuit_BlackBox_Model.pdf
  - Example is for a Tx circuit that includes an FFE.
  - The circuit is characterized as a black box with input/output waveform data over the circuit parameter states for three corner cases.
  - The SerDesDesign.com Channel Simulator is used: serdes-system-single-channel-tool

Typical Rx Models

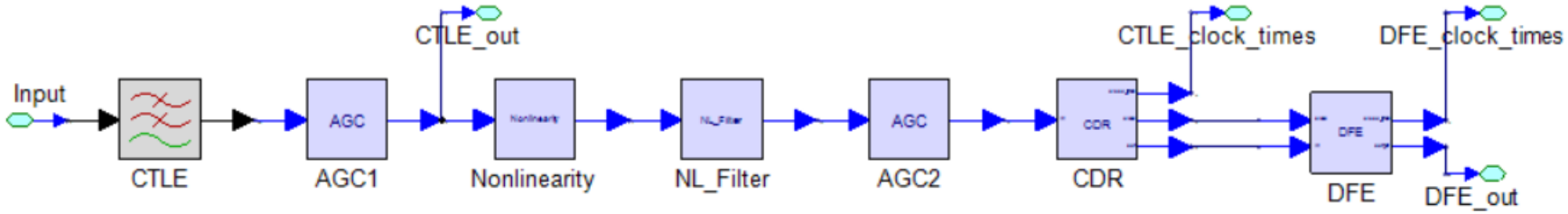
- The SerDes system Rx circuit is modeled as a Rx IBIS-AMI model per the IBIS-AMI standard with an AMI portion and an IBIS portion as shown here.



- The Rx IBIS Buffer characteristic is included into the total single ended impulse response between the Tx_AMI and Rx_AMI models.
- Conceptually, the Rx IBIS portion takes an input differential signal and outputs a single ended signal. The Rx AMI model receives that single ended signal and outputs a modified single ended signal.
- The Rx AMI typically contains a linear CTLE, a nonlinearity, clock and data recovery (CDR) block and DFE (decision feedback equalizer) and is NLTV.
- The Rx AMI model can also be LTI.
  - For the Channel Simulator Statistical mode, the Rx LTI model converts its input impulse response to an output impulse response.

Typical Rx Models

- The are many options for modeling a SerDes Rx circuit; a few are highlighted here.
  - All Rx models can have output jitter defined (Rj, Dj, DCD, Sj/SjFreq).
- In general, the SerDesDesign.com built-in Rx model has this form:



- Any of the component parts can be used seperately or in combination.
- The CTLE can be LTI or NLTV and can have 1, 2, 3 or 4 stages.
  - The CTLE can have its states auto optimized for best output eye metrics.
- A 1-stage CTLE can be defined:
  - As an AGC only
  - With a set of step responses or spectrums
  - With a set of poles and zeros or set of peaking frequencies and peaking dBs.

Typical Rx Models

- A 2-stage CTLE can be defined:
  - With a set of step responses for each stage.
  - With the two stages in parallel or in series.
  - Two parallel stages have the input signal split between the two stages and the split ratio can be auto optimized for best output eye metrics.
- A 2 or 4 stage CTLE:
  - Is defined with a set of step responses for each stage.
- For all CTLEs:
  - An LTI model has its optimal states set during model initialization by statistical analysis of the input impulse response.
  - An NLTV model has its optimal states set during model run-time by waveform analysis after a defined number of ignore symbols.
- The AGC block can be LTI or NLTV.
  - The LTI AGC set the AGC gain during model initialization by statistical analysis of the input impulse response.
  - An NLTV model has its optimal states set during model run-time by waveform analysis after a defined number of ignore symbols.

Typical Rx Models

- The Nonlinearity can be defined:
  - 1. With a Tanh() nonlinear function.
  - 2. With a Rapp type of nonlinearity.
  - 3. With table data (vout vs vin)
  - 4. With a set of vout/vin tables that are coordinated with the state of the last stage of the CTLE.
- The Nonlinearity filter can be defined:
  - With a set of poles.
  - With step response data.
  - With a set of step response data whose selection is coordinated with the nonlinearity selected from NonlinearityType=4 (a set of vout/vin tables).
- The CDR is a Bang-Bang type of CDR
  - Its timing phase is automatically set for optimal input waveform sampling instant.
  - The timing phase can be adjusted by the user.
  - The user can specify the corner frequency (Fc) for the observed jitter transfer function (OJTF).

Typical Rx Models

- The DFE can be defined:
  - With any number of taps.
  - With tap values specified.
  - With upper and lower limits set for the taps.
  - With the taps defined a quantized states from a min to max with specified tap size and with the taps selected with a tap code.
  - With the tap delays defined with values other than 1 UI delay.
  - With the option for the taps to be optimized at initialization and and option for the taps to continuously adapt during run-time.
- All Rx models can have an optional output CompensationFilter as needed to get a better waveform match to a reference Spice simulated reference waveform.

Typical Rx Models

- Example for an Rx circuit.
  - Documentation: SerDesDesign_Example_Rx_Circuit_Model.pdf
  - Example is for a Rx circuit that includes a CTLE, AGC, CDR and DFE.
  - The CTLE is LTI and characterized using circuit input/output waveform data over the CTLE parameter states.
  - The DFE is characterized based on typical circuit DFE parameters and uses the built-in SerDesDesign.com DFE model.
  - The CDR is characterized based on typical circuit CDR Observed Jitter Transfer Function corner frequency (OJTF Fc) and uses the built-in SerDesDesign.com CDR model.
  - The SerDesDesign.com Channel Simulator is used: serdes-system-single-channel-tool

Some Channel Simulation Features

- Independently defined waveforms for waveform display and for detail eye/BER analysis.
- Supports overlaying the total channel impulse response s21dd characteristic over the total channel band-limited s21dd characteristic.
- Automatically sets the Bit-by-Bit mode histogram amplitude levels.
- Supports use of multiple processors in parallel to achieve Channel Simulation times that can be faster by a 10x factor or more when simulating 10M or more UI's.
- Supports detail eye analysis as a post processing feature on the Channel Simulation Bit-by-Bit mode statistical histogram data base; including resetting the eye slicing levels for amplitude and time, specifying additional timing jitter (Rj, Dj, DCD, Sj).
- Supports overlaying the time/amplitude extrapolated BER plots over the raw data BER plots.

Some Channel Simulation Features

- Supports re-use of the total channel h21dd impulse response in new Channel Simulations so that the total channel impulse need not be regenerated for the same total channel.
- Supports generating Tx and Rx IBIS-AMI models and SystemVue models for Channel Simulations using built-in Tx and Rx models.
- Supports custom IBIS-AMI Modeling training for user customization of the source code provided for their custom IBIS-AMI models.
- Supports providing customers a custom Linux build machine with a fully loaded build environment including their custom IBIS-AMI model software.

Some Custom Modeling Features

- Besides the Tx, channel and Rx model built into SerDesDesign.com, many custom models have been delivered to customers including:
- Tx black box models for a Tx circuit with a 3 tap FFE with 4096 FFE states and with the Tx IBIS buffer de-embedded from the Tx data.
- Rx models for a CTLE with 4 stages with additional nonlinearities and AGC.
- PAM4 Tx/Rx models at over 25 GBaud per second.
- Tx/Rx models per the IBIS 7.0 standard that include Rx to Tx back channel communication and use S4P files for the IBIS buffer representation.
- Redriver/Retimer models for electro-optical systems.
- Optical VCSEL driver models with different rise and fall waveform characteristics based on EO hardware waveform measurements.
- DDR models with different rise and fall waveform characteristics.
- DDR models using a CDR with arbitrary user specified Observer Jitter Transfer Function data versus frequency.

Appendix

IBIS-AMI Modeling Flow

- Use SerDesDesign.com for IBIS-AMI model development.
- Construct the IBIS-AMI models in the SerDes Systems Tool
  - https://www.serdesdesign.com/home/serdes-system-single-channel-tool
  - Iterate as needed to achieve desired performance.
- Generate the Tx or Rx IBIS-AMI model from the web site.
  - Typical cost is as low as $2K per model.
- There is no need for the IBIS-AMI model developer to be an expert on the IBIS standard, C/C++ coding, or in setting up the compile and linking rules in the Microsoft Visual Studio or Linux tools.
- IBIS-AMI Tx and Rx models generated from SerDesDesign.com can used in any Channel Simulator.