Subject: Channel Simulation MultiCore Calibration Tests

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This paper discusses Channel Simulation features available on the web site:
https://www.serdesdesign.com/

Introduction

Serdesdesign.com is used to perform Channel Simulation tests on SerDes system per the IBIS-AMI standard (**https://ibis.org**). Serdesdesign.com was used to perform Channel Simulation tests using up to 28 CPU Cores with parallel processing. For a defined typical SerDes system, Channel Simulation timing metrics were collected as a function of the number of Analysis Bits and Number of Cores.

Test Hypothesis: The SerDes system BER performance is constant regardless of the number of Analysis Bits (above a minimum) used and the Number (N) of Cores (up to a maximum) used while achieving an analysis time reduction by up to a factor of N (the Number of Cores used). The greater the N, the greater the analysis time reduction without compromising the system BER performance.

Conclusion: The tests performed validate this hypothesis. Thus, no system performance is compromised when multiple Cores are used and can provide up to 23 times reduction (for N = 28) in the system analysis time.

This report documents these test metrics.

As defined, the above hypothesis is not the key value in delivering multiprocessor based Channel Simulation. Rather, validation of the test hypothesis shows that the SerDesDesign.com Channel Simulation results are correct when multiprocessors are used.

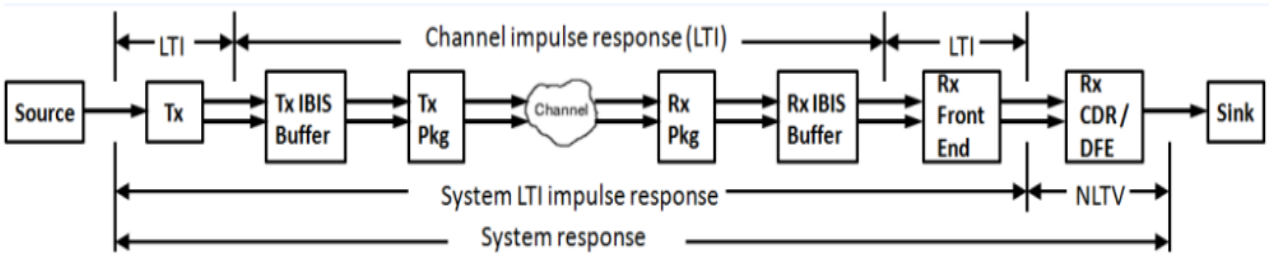
The real value of Channel Simulation with multiprocessors is realized when the SerDes system is defined with the use of transmit timing jitter (deterministic, Gaussian, etc.). Tests with timing jitter for Channel Simulation with multiprocessors is discussed in separate reports.

Additional reference reports:

- Channel_Simulation_BER_Extrapolation.pdf
  - Documents discussion of the Channel Simulation use of BER extrapolation.
- Channel_Simulation_NRZ_System_MultiCore_Tests.pdf
  - Documents Channel Simulation MultiCore tests using NRZ data.
- Channel_Simulation_PAM4_System_MultiCore_Tests.pdf
  - Documents Channel Simulation MultiCore tests using PAM4 data.

The Defined Typical SerDes System

A typical single channel SerDes system is defined in this block diagram.



The typical test case is defined with these characteristics:

Source: NRZ data with 25.78 Gbps bit rate using 32 samples per bit and PRBS register length = 15 bits.

Tx: AMI portion of a custom Tx IBIS-AMI model with FFE with 3 quantized taps and filtering

- Typical corner case used.
- Cm1 (pre-cursor) code and Cm (post-cursor) code were set to their optimal states for the given total channel.

Tx IBIS Buffer: IBIS portion of this IBIS-AMI model.

Tx Pkg: 4 port differential S-parameter file

Channel: 4 port differential S-parameter file

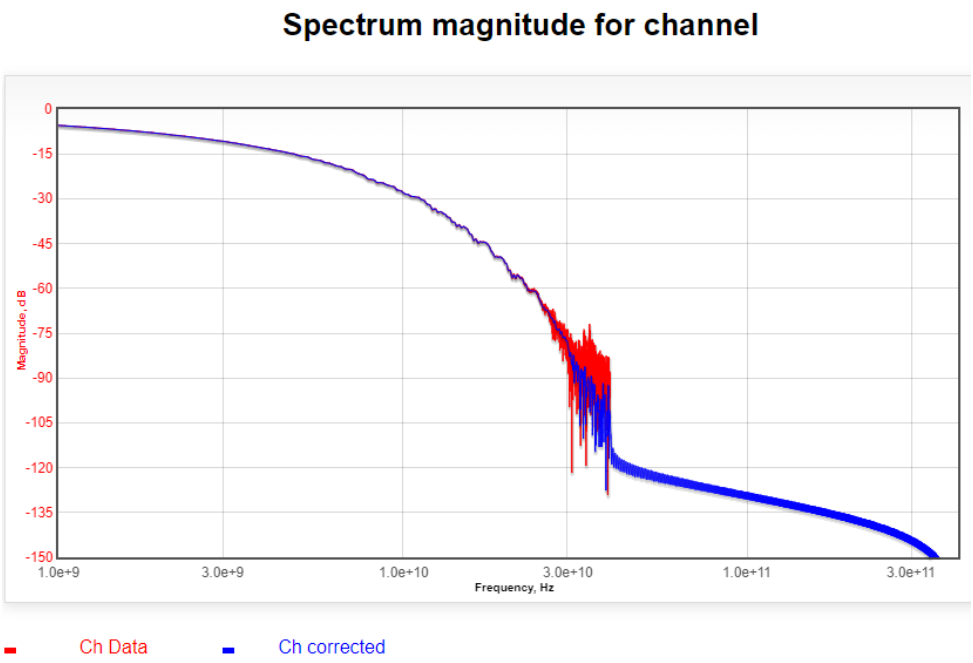
Rx Pkg: 4 port differential S-parameter file

Rx IBIS Buffer: IBIS portion of the Rx IBIS-AMI model.

Rx Front End/CDR/DFE: AMI portion of a custom Rx IBIS-AMI model with 4 stage continuous time linear equalizer (CTLE), Nonlinearity, CDR and DFE with 5 quantized taps.

- Typical corner case
- 4 stage CTLE states were set to their optimal states for the given total channel + Tx.
- 5 tap DFE taps were initialized to their optimal states and continuously adapted.
- Ignore_Bits = 20,000; defines the maximum initial startup transient after which the AnalysisBits are recorded.

The total channel is composed of the cascade of Tx IBIS Buffer + Tx Pkg + Channel + Rx Pkg + Rx IBIS Buffer and has 34 dB loss at Nyquist. For the timing metrics, the total channel is represented by its h21dd impulse response with this differential (h21dd) frequency domain characteristic:



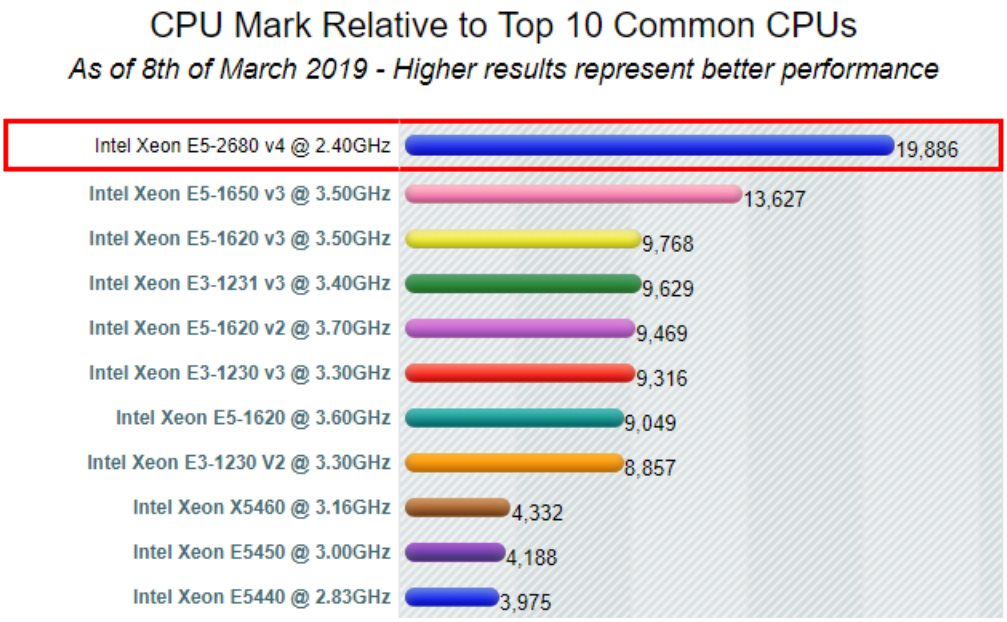
Ch Data (red): Represents the raw S-parameter data that includes non-physical characteristics such as noise and non-causality.

Ch Corrected (blue): Represents the S-parameters corrected to remove non-physical characteristics such as noise and non-causality.

Server CPU Characteristics

The 64 bit Linux server uses the CentOS 6.10 Linux Operating System, has 28 Cores and uses this CPU: Intel 2x Xeon E5-2680v4 - 28c/56t - 2.4GHz /3.3GHz

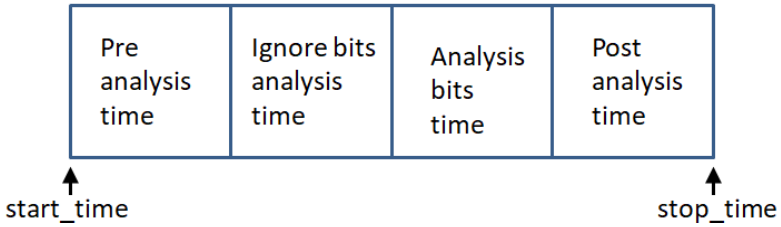
This CPU has the following benchmark as reported by PassMark (https://www.cpubenchmark.net).



As can be seen, this CPU used is rated top in its class.

Defining the Run Time Metrics

The SerDes Channel Simulation has run time metrics composed of these 4 sequential parts:



The Pre_analysis_time is the time it takes for the analysis to be set up during the run time.

This time is constant as the number of cores or the number of analysis bits increases.

The Ignore_bits_time is the analysis start up transient time for the defined ignore bits.

This time is constant as the number of cores or the number of analysis bits increases.

The Analysis_bits_time is the analysis time for the actual analysis bits.

This time decreases slightly less than 1/N where N = the number of cores.

A decrease of 1/N is ideal with full efficiency in partitioning the job among the N cores.

The Post_analysis_time is the time after the analysis for post processing the analysis results.

This time is constant as the number of cores or the number of analysis bits increases.

The Overhead_time = Pre_analysis_time + Ignore_bits_time + Post_analysis_time

Let AnalysisBits = the number of bits to analyze.

Let NumCores = the number of cores used.

Let PRBS_Len = the number of register bits in the Source Pseudo Random Sequence generator.

- PRBS_Len = 15 is used in these tests.

PRBS_Bits = 2^(PRBS_Len) - 1 = the actual number of bits in the PRBS sequence.

- PRBS_Bits = 32767 in these tests.

iAnalysisBits[i] = the number of analysis bits assigned to each core for i = 0 to NumCores-1.

iAnalysisBits[i] = PRBS_Bits*int(AnalysisBits/PRBS_Bits/NumCores); for i = 0 to i<NumCores-2

iAnalysisBits[NumCores-1] = AnalysisBits - (NumCores-2)* iAnalysisBits[0]; for i = NumCores-1

Ideal time = N * iAnalysisBits[0]

- Ideal time vs N will be a straight line when plotted with log10(time) vs log10(N).

Expected time = N * iAnalysisBits[0] + Overhead_time

- Expected time vs N will be offset from the ideal line when plotted with log10(time) vs log10(N).

Actual time = Total_overhead_time + Analysis_bits_time

- Actual time vs N will track Expected time when N is low, but will deviate from the Expeced time as N increases, especially for larger values of AnalysisBits. This is due to the additional time required for the multi-core communication and data coordination.

For the defined SerDes system, simulations are run with these values of AnalysisBits and NumCores.

- AnalysisBits = 131,072; 1,048,576; 16,777,216
- NumCores = 1, 2, 4, 8, 16
  - The MaxNumCores used is limited as a function of AnalysisBits and PRBS_Len to iAnalysisBits[i] listed above.
  - MaxNumCores = 2; for AnalysisBits = 131, 072
  - MaxNumCores = 4; for AnalysisBits = 1,048,576

- MaxNumCores = 16; for AnalysisBits = 16,777,216

The timing metrics are recorded as a function of AnalysisBits and NumCores.

- Timing metrics: Ideal time, Expected time, Actual time
- BER performance

MaxNumCores vs AnalysisBits and PRBS_Len

Using the expressions in the previous section, the following tables show the MaxNumCores versus AnalysisBits as the PRBS register length is varied from 12 to 30. The AnalysisBits listed are at powers of 2 values.

The relationships shown in these tables assures that there is no statistical noise when combining the results from the multiple Cores.

The SerDesDesign.com web site allows a user to override these relationships and select any number of Cores for the specified AnalysisBit and PRBS_Len value at some cost in statistical noise when combining the results from the multiple Cores.

2^N	AnalysisBits	PRBS_Len = 12 MaxNumCores	PRBS_Len = 13 MaxNumCores	PRBS_Len = 14 MaxNumCores	PRBS_Len = 15 MaxNumCores	PRBS_Len = 16 MaxNumCores
17	131,072	4	4	4	2	2
18	262,144	9	4	4	4	2
19	524,288	14	9	4	4	4
20	1,048,576	17	14	9	4	4
21	2,097,152	17	17	14	9	4
22	4,194,304	25	17	17	14	9
23	8,388,608	28	25	17	17	14
24	16,777,216	28	28	25	17	17
25	33,554,432	28	28	28	25	17
26	67,108,864	28	28	28	28	25
27	134,217,728	28	28	28	28	28
28	268,435,456	28	28	28	28	28
29	536,870,912	28	28	28	28	28
30	1,073,741,824	28	28	28	28	28

2^N	AnalysisBits	PRBS_Len = 17 MaxNumCores	PRBS_Len = 18 MaxNumCores	PRBS_Len = 19 MaxNumCores	PRBS_Len = 20 MaxNumCores	PRBS_Len = 21 MaxNumCores
17	131,072	1	1	1	1	1
18	262,144	2	1	1	1	1
19	524,288	2	2	1	1	1
20	1,048,576	4	2	2	1	1
21	2,097,152	4	4	2	2	1
22	4,194,304	4	4	4	2	2
23	8,388,608	9	4	4	4	2
24	16,777,216	14	9	4	4	4
25	33,554,432	17	14	9	4	4
26	67,108,864	17	17	14	9	4
27	134,217,728	25	17	17	14	9
28	268,435,456	28	25	17	17	14
29	536,870,912	28	28	25	17	17
30	1,073,741,824	28	28	28	25	17

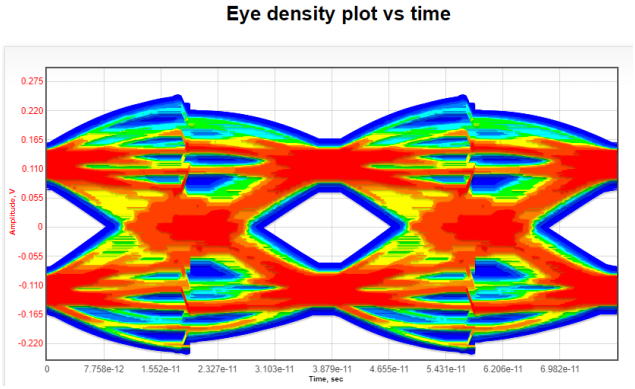
2^N	AnalysisBits	PRBS_Len = 22 MaxNumCores	PRBS_Len = 23 MaxNumCores	PRBS_Len = 24 MaxNumCores	PRBS_Len = 25 MaxNumCores	PRBS_Len = 26 MaxNumCores

17	131,072	1	1	1	1	1
18	262,144	1	1	1	1	1
19	524,288	1	1	1	1	1
20	1,048,576	1	1	1	1	1
21	2,097,152	1	1	1	1	1
22	4,194,304	1	1	1	1	1
23	8,388,608	2	1	1	1	1
24	16,777,216	2	2	1	1	1
25	33,554,432	4	2	2	1	1
26	67,108,864	4	4	2	2	1
27	134,217,728	4	4	4	2	2
28	268,435,456	9	4	4	4	2
29	536,870,912	14	9	4	4	4
30	1,073,741,824	17	14	9	4	4

2^N	AnalysisBits	PRBS_Len = 27 MaxNumCores	PRBS_Len = 28 MaxNumCores	PRBS_Len = 29 MaxNumCores	PRBS_Len = 30 MaxNumCores
17	131,072	1	1	1	1
18	262,144	1	1	1	1
19	524,288	1	1	1	1
20	1,048,576	1	1	1	1
21	2,097,152	1	1	1	1
22	4,194,304	1	1	1	1
23	8,388,608	1	1	1	1
24	16,777,216	1	1	1	1
25	33,554,432	1	1	1	1
26	67,108,864	1	1	1	1
27	134,217,728	1	1	1	1
28	268,435,456	2	1	1	1
29	536,870,912	2	2	1	1
30	1,073,741,824	4	2	2	1

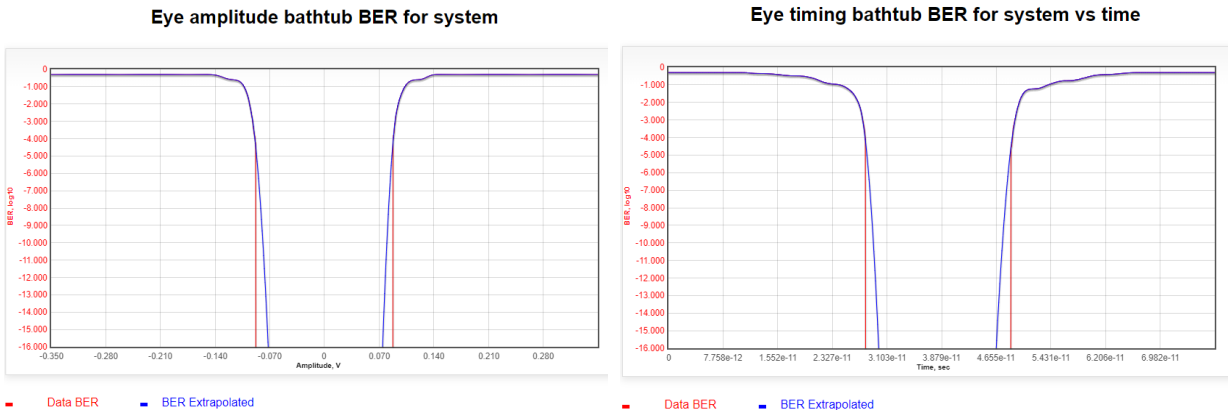
Typical SerDes System Characteristics

Using Bit-by-Bit Analysis, AnalysisBits = 131, 072 bits, PRBS bit register length = 15 and using 1 Core, the system has these results for eye density diagram and BER plots:



Observe that the eye level is within -0.25 V and +0.25 V and the nominal single sided eye height is 0.125 V.

Here are the BER plots with no Tx timing jitter:



Observe that the "Data BER" plot is accurate down to 10^(-4.5) with is approximately equal to 1/PRBS_Bits = 1/(32,767). The "BER Extrapolated" plot uses extrapolation to obtain the BER at lower levels.

The following metrics are discussed with no Tx timing jitter.

Run Time Metrics with No Tx Timing Jitter

For each AnalysisBits, these timing metrics are shown for each NumCores:

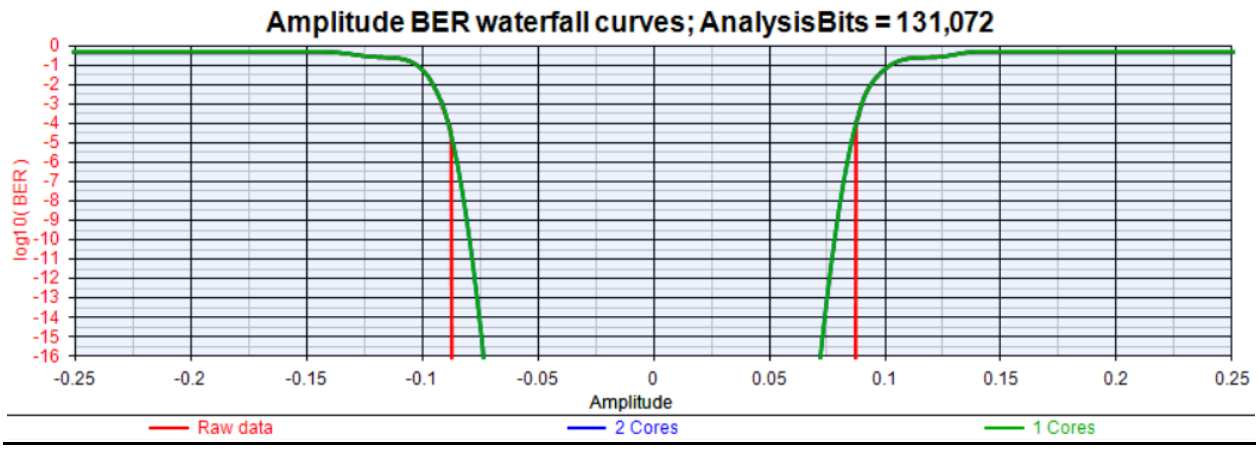
- Ideal; ideal run time with no overhead time.
- Expected: expected run time with constant overhead time.
- Actual: actual recorded run time
- BER metrics: amplitude and timing BER waterfall curves.

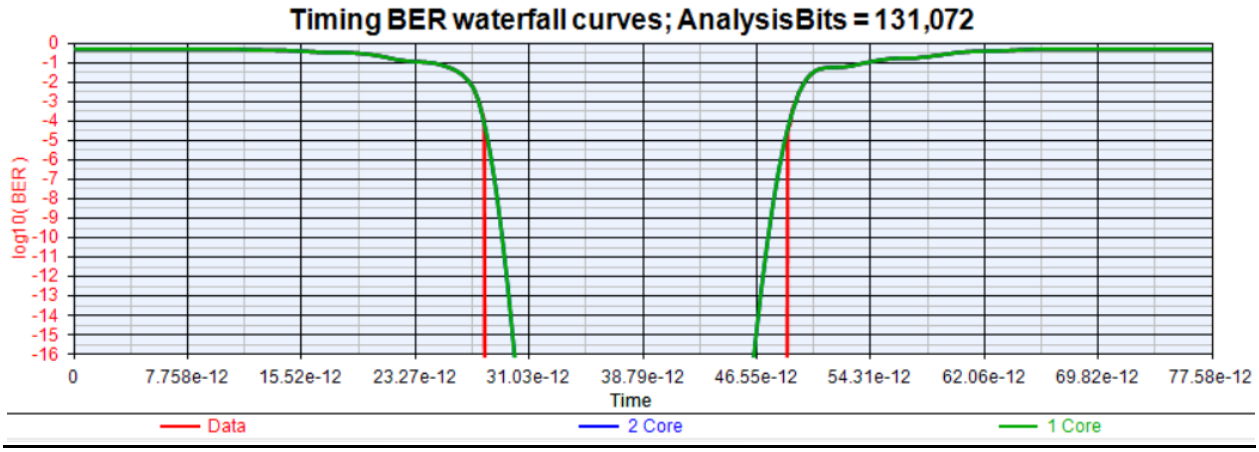
Comment: Since there is no Tx timing jitter, the only jitter is data dependent jitter. Since the PRBS sequence repeats itself, the BER curves are expected to be the same for any of the tested AnalysisBits for any number of cores.

AnalysisBits = 131,072; NumCores = 1, 2

AnalysisBits	131,072	Overhead	21.000
#Cores	Ideal	Expected	Actual
1	72.00	93.000	93.000
2	36.00	57.000	57.000

Observation: The expected and actual times match exactly.



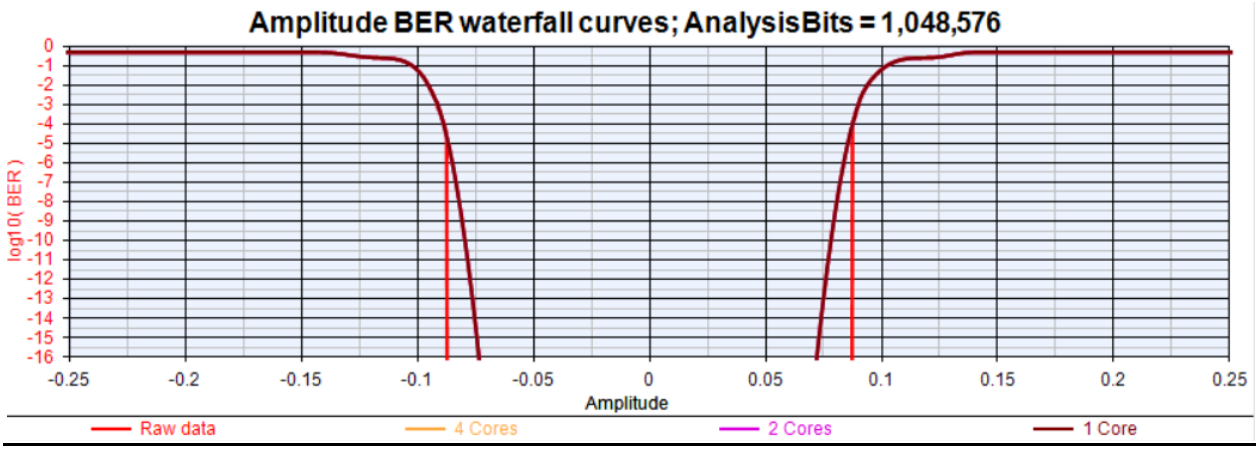


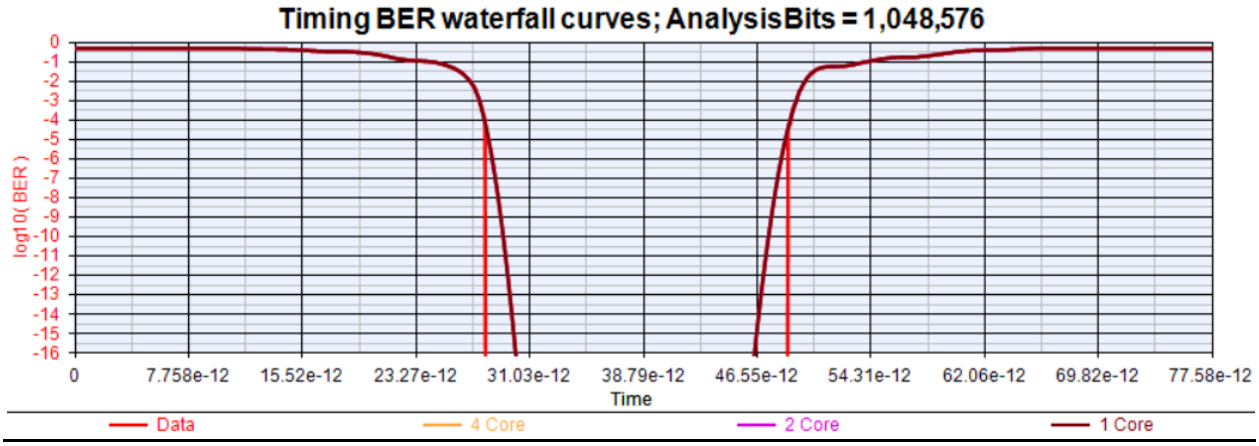
Observation: These BER curves show that **results with 1 and 2 Cores overlap perfectly as expected**.

AnalysisBits = 1,048,576; NumCores = 1, 2, 4

AnalysisBits	1,048,576	Overhead	21.000
#Cores	Ideal	Expected	Actual
1	574.00	595.000	595.000
2	287.00	308.000	308.000
4	143.50	163.500	168.000

Observation: The expected and actual times match very good with the actual with 4 cores having a slight increase above the expected value.





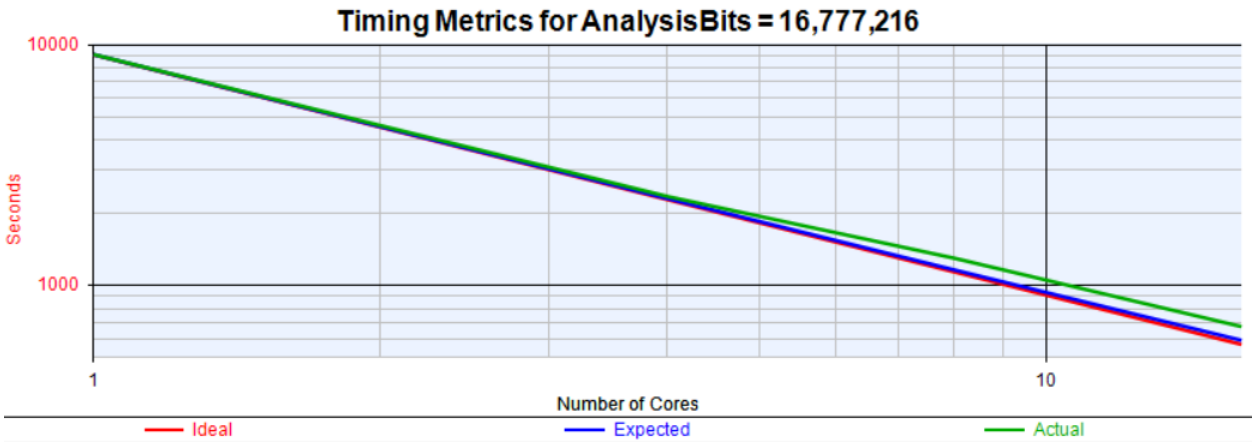
Observation: These BER curves show that the **results with 1, 2 and 4 Cores overlap perfectly as expected**.

AnalysisBits = 16,777,216; NumCores = 1, 2, 4, 8, 16

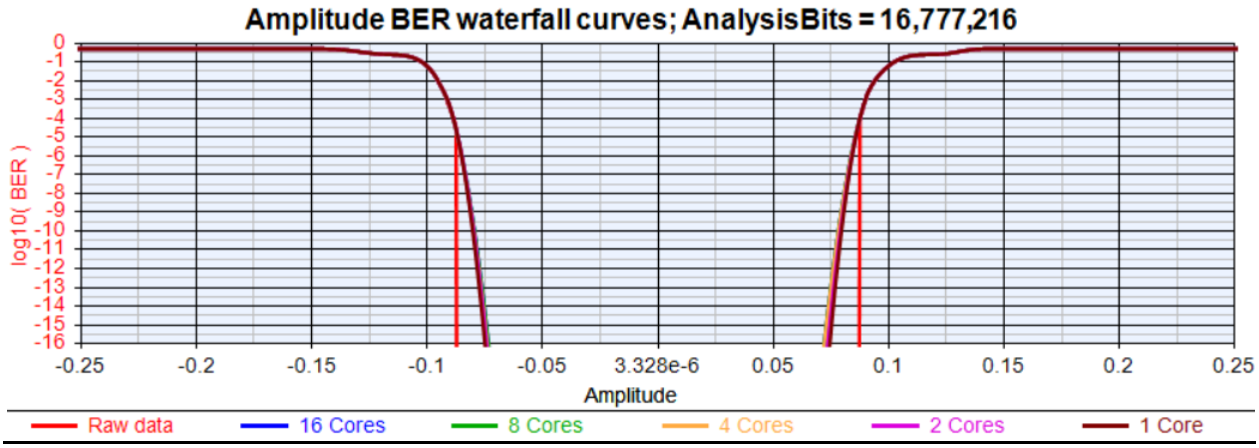
AnalysisBits	16,777,216	Overhead	21.000
#Cores	Ideal	Expected	Actual
1	9096.00	9117.00	9117.00
2	4548.00	4569.00	4620.00
4	2274.00	2295.00	2343.00
8	1137.00	1158.00	1297.00
16	568.50	589.50	674.00

Observation: The actual times increase above the expected times as the number of cores increases. This is as expected for the larger AnalysisBits tests. With 16 Cores, the run time is reduced by a factor of 13.5x from that with the use of 1 Core.

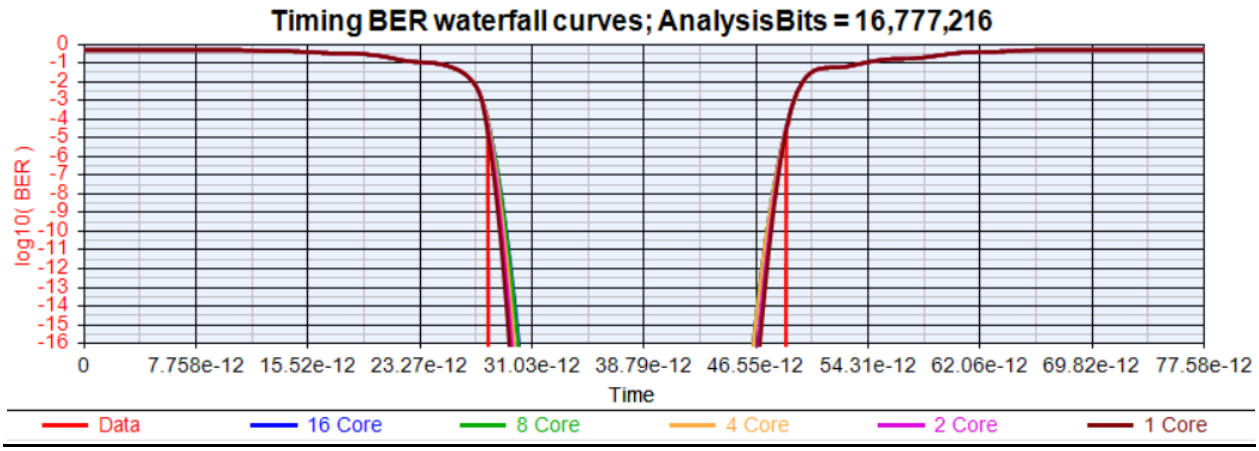
This tabular data is shown graphically in this chart with log(time) for the y-axis and log(number of cores) for the x-axis:



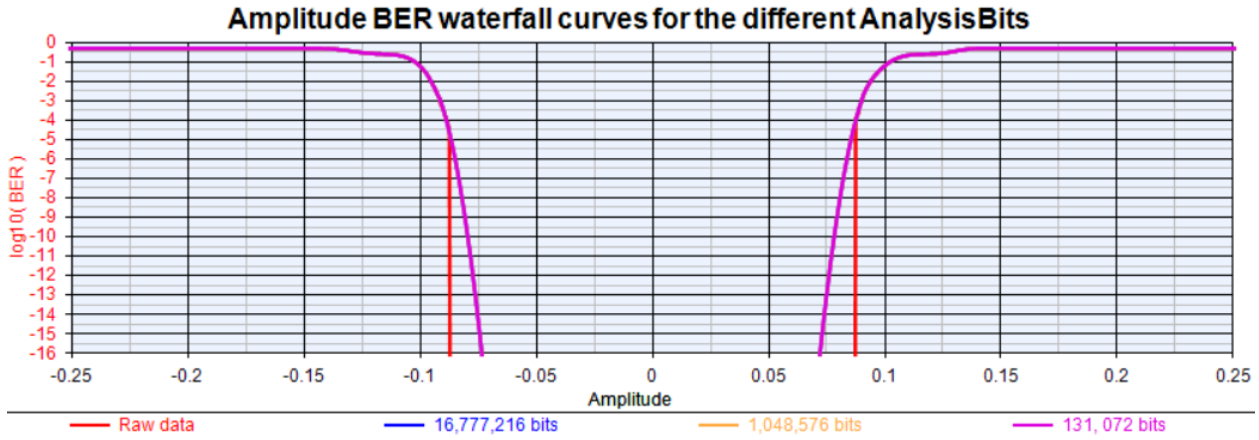
Observation: The Ideal curve is a straight line. The Expected curve deviates from the Ideal as a result of the additional constant Overhead_time. The Actual curve deviates from the Expected as Number of Cores increases by an amount that is attributed to the incremental increase in the time for multi-core communication and processing.



Observation: The Amplitude BER curves show that the Cores result in a very good match. There is a lot of processing to extract these extrapolated BER curves from the raw data that produces the eye density data. Thus, the difference is presumed to be due to processing noise 1) for the much larger number of AnalysisBits and 2) for the extrapolation below 10^(-5) .

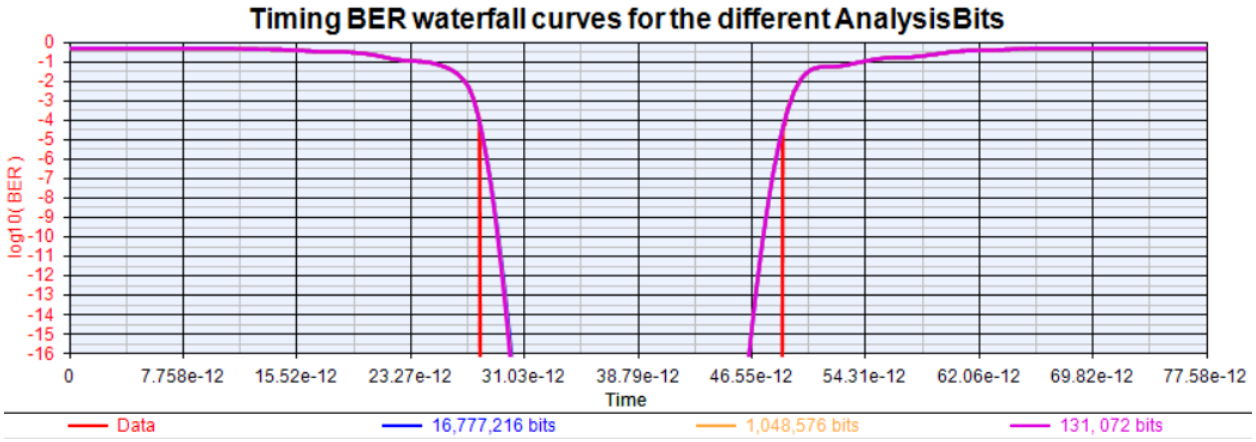


Observation: The Timing BER curves show that the Cores result in a very good match though not as good as the Amplitude BER curves. These timing extrapolated BER curves are based on further processing the data from the amplitude BER curves, which already requires a lot of processing to extract from the raw data that produces the eye density data. Thus, the difference is presumed to be due to the even more processing noise.



Observations:

- The Raw data is the same no matter what AnalysisBits or number of Cores is used, as expected.
- The BER for 131,072 bits is with 2 Cores.
- The BER for 1,048,576 bits is with 4 Cores.
- The BER for 16,777,216 bits is with 16 Cores.
- For this test case, **all three BER curves overlap identically, as expected**.



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- The BER for 16,777,216 bits is with 16 Cores.
- For this test case, **all three BER curves overlap identically, as expected**.

Summary results for AnalysisBits = 134,217,728; NumCores = 1 and 16

With 28 Cores, the run time is reduced by a factor of 23x from that with the use of 1 Core.

Conclusion for Run Time Metrics with No Tx Timing Jitter

The above tests validate the test hypothesis that when the SerDes system has no additive jitter or noise, then the system BER performance is constant regardless of the number of Analysis Bits (above a minimum) and the Number of Cores (up to a maximum) used.

Thus, the system performance is not compromised when multiple Cores are used and can provide up to 23x reduction in the system analysis time.