Subject: Channel Simulation NRZ System MultiCore Tests
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This paper discusses Channel Simulation features available on the web site:
https://www.serdesdesign.com/

Introduction

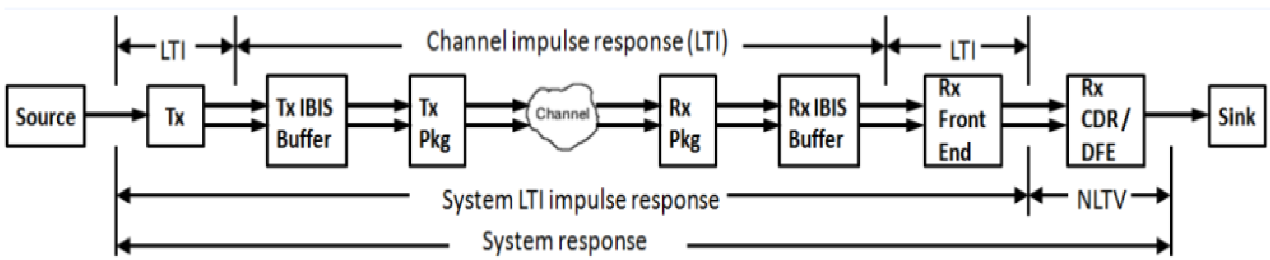
Serdesdesign.com is used to perform Channel Simulation tests on SerDes system per the IBIS-AMI standard (https://ibis.org). Serdesdesign.com was used to perform Channel Simulation tests using up to 28 CPU Cores with parallel processing. For a defined typical SerDes system using NRZ data, Channel Simulation timing metrics were collected as a function of the number of Analysis Bits and Number of Cores.

This report is documents these test metrics.

Additional reference reports:
- Channel_Simulation_BER_Extrapolation.pdf
  - Documents discussion of the Channel Simulation use of BER extrapolation.
- Channel_Simulation_MultiCore_Calibration_Tests.pdf
  - Documents description of the MultiCore CPU, definition of the analysis run time metrics, and BER metrics when no timing jitter is used.
- Channel_Simulation_PAM4_System_MultiCore_Tests.pdf
  - Documents Channel Simulation MultiCore tests using PAM4 data.

The Defined Typical SerDes System

A typical single channel SerDes system is defined in this block diagram.



Source: NRZ data with 25.78 Gbps bit rate using 32 samples per bit and PRBS register length = 15 bits.

Tx: AMI portion of a custom Tx IBIS-AMI model with FFE with 3 quantized taps and filtering

- Typical corner case

- Cm1 (pre-cursor) code and Cm (post-cursor) code were set to their optimal states for the given total channel.
- Transmit Gaussian timing jitter: Tx_Rj = 0.287e-12 sec.
- Transmit Deterministic timing jitter: Tx_Dj = 1.76e-12 sec.
- Transmit Duty Cycle Distortion jitter: Tx_DCD = 0.19e-12 sec.

Tx IBIS Buffer: IBIS portion of this IBIS-AMI model.

Tx Pkg: 4 port differential S-parameter file

Channel: 4 port differential S-parameter file

Rx Pkg: 4 port differential S-parameter file

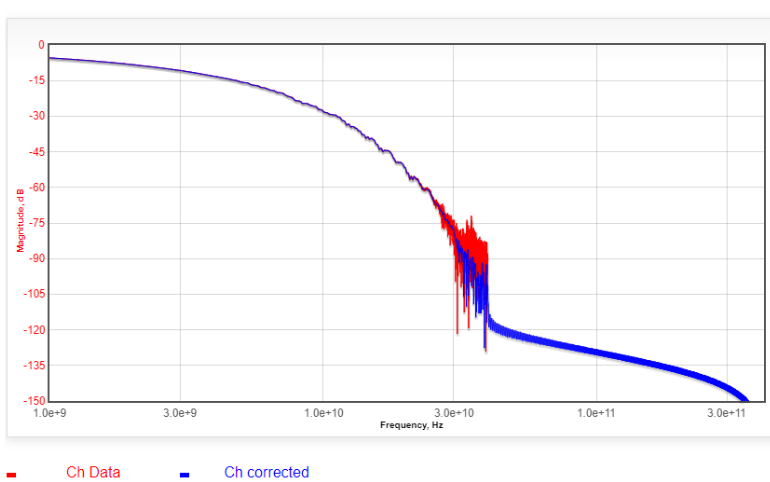
Rx IBIS Buffer: IBIS portion of the Rx IBIS-AMI model.

Rx Front End/CDR/DFE: AMI portion of a custom Rx IBIS-AMI model with 4 stage continuous time linear equalizer (CTLE), Nonlinearity, CDR and DFE with 5 quantized taps.

- Typical corner case
- 4 stage CTLE states were set to their optimal states for the given total channel + Tx.
- 5 tap DFE taps were initialized to their optimal states and continuously adapted.
- Ignore_Bits = 20,000; this defines the maximum initial startup transient after which the AnalysisBits are recorded.

The total channel is composed of the cascade of Tx IBIS Buffer + Tx Pkg + Channel + Rx Pkg + Rx IBIS Buffer and has 34 dB loss at Nyquist. For the timing metrics, the total channel is represented by its h21dd impulse response with this differential (h21dd) frequency domain characteristic:

Spectrum magnitude for channel



Ch Data (red): Represents the raw S-parameter data that includes non-physical characteristics such as noise and non-causality.

Ch Corrected (blue): Represents the S-parameters corrected to remove non-physical characteristics such as noise and non-causality.

For the defined SerDes system, simulations are run with these values of AnalysisBits and NumCores.

- AnalysisBits = 131,072; 1,048,576; 16,777,216
- NumCores = 1, 2, 4, 8, 16
    - MaxNumCores = 2; for AnalysisBits = 131, 072
    - MaxNumCores = 4; for AnalysisBits = 1,048,576
    - MaxNumCores = 16; for AnalysisBits = 16,777,216

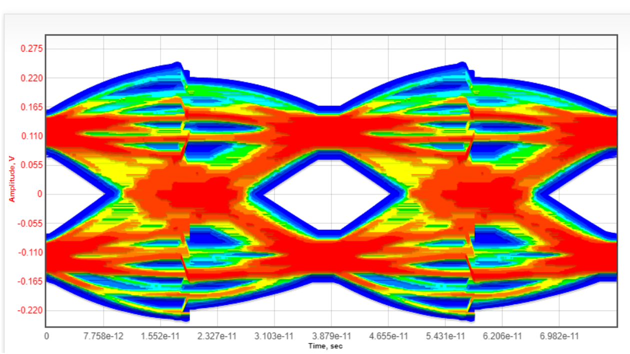
The timing metrics are recorded as a function of AnalysisBits and NumCores.

- Timing metrics: Ideal time, Expected time, Actual time
- BER performance

Typical SerDes System Characteristics

Using Bit-by-Bit Analysis, AnalysisBits = 131, 072 bits and PRBS bit register length = 15 the system has these results for eye density diagram and BER plots:

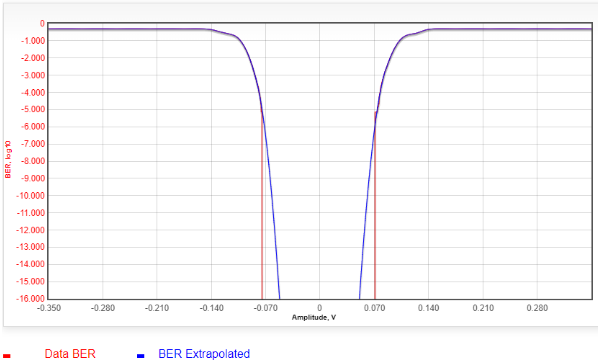
Eye density plot vs time



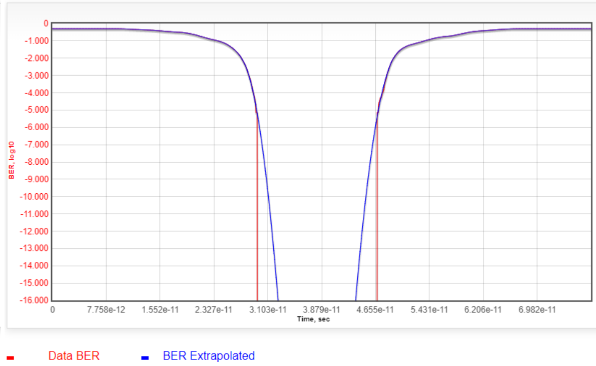
Observe that the eye level is within -0.25 V and +0.25 V and the nominal single sided eye height is 0.125 V.

Here are the BER plots when the Tx timing jitter is enabled:

Eye amplitude bathtub BER for system



Eye timing bathtub BER for system vs time



Observe that the "Data BER" plot is accurate down to 10^(-5) with is approximately equal to 1/AnalysisBits = 1/(131, 072). The "BER Extrapolated" plot uses extrapolation to obtain the BER at lower levels.

Metrics are discussed with Tx timing jitter enabled.

Run Time Metrics with Tx Jitter Enabled

For each AnalysisBits, these timing metrics are shown for each NumCores:

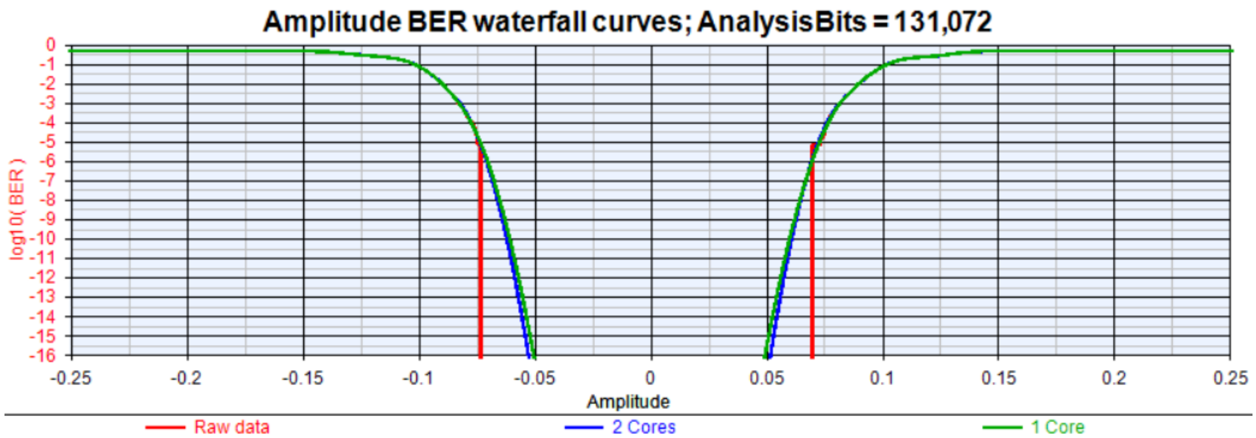
- Ideal; ideal run time with no overhead time.
- Expected: expected run time with constant overhead time.
- Actual: actual recorded run time
- BER metrics: amplitude and timing BER waterfall curves.

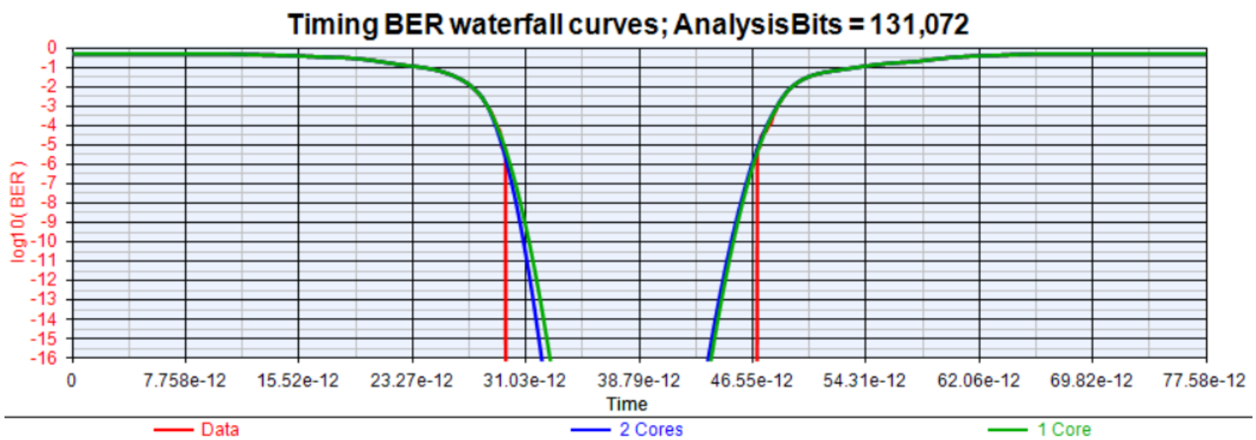
Comment: Tx timing jitter is based on the use of random number generators. For each simulation run, different random numbers are used. Thus, for each simulation run, it is expected that the BER results will have some variation due to the differences in the Tx timing jitter for each run.

AnalysisBits = 131,072; NumCores = 1, 2

AnalysisBits	131,072	Overhead	21.000
#Cores	Ideal	Expected	Actual
1	74.00	95.000	95.000
2	37.00	58.000	58.000

Observation: The expected and actual times match exactly.



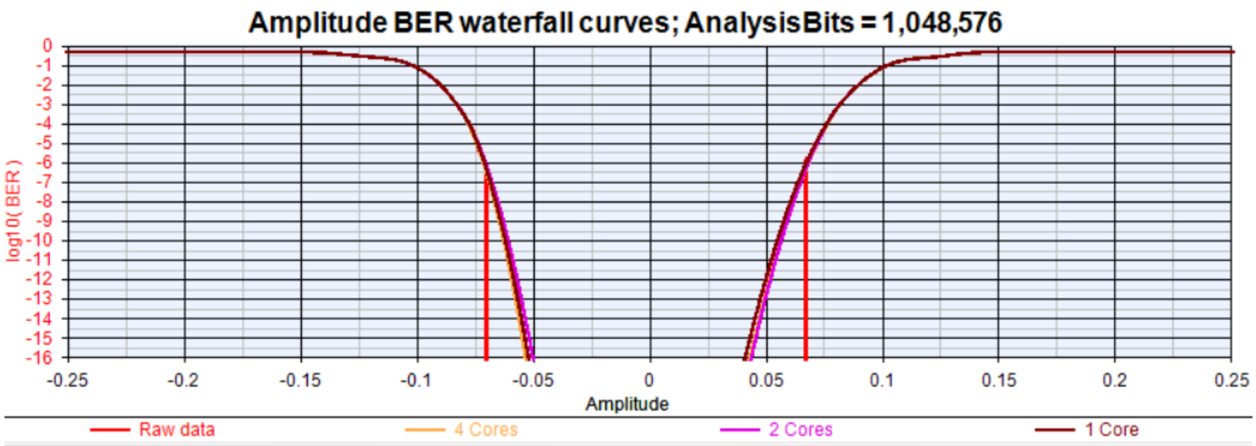


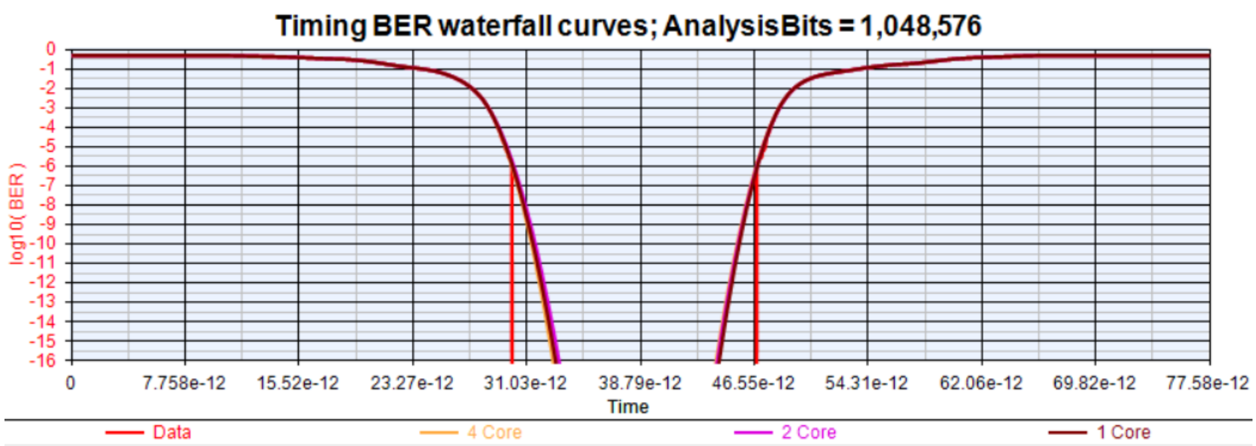
Observation: All BER curves are equally valid. Since it is known that the jitter statistics are different for each simulation, it is understood that the Extrapolated BER curves with have some variation.

AnalysisBits = 1,048,576; NumCores = 1, 2, 4

AnalysisBits	1,048,576	Overhead	20.000
#Cores	Ideal	Expected	Actual
1	587.00	607.000	607.000
2	293.50	313.500	318.000
4	146.75	166.750	170.000

Observation: The actual times track the expected times, but with the actual values for 2 or 4 cores having a slight increase above the expected values.





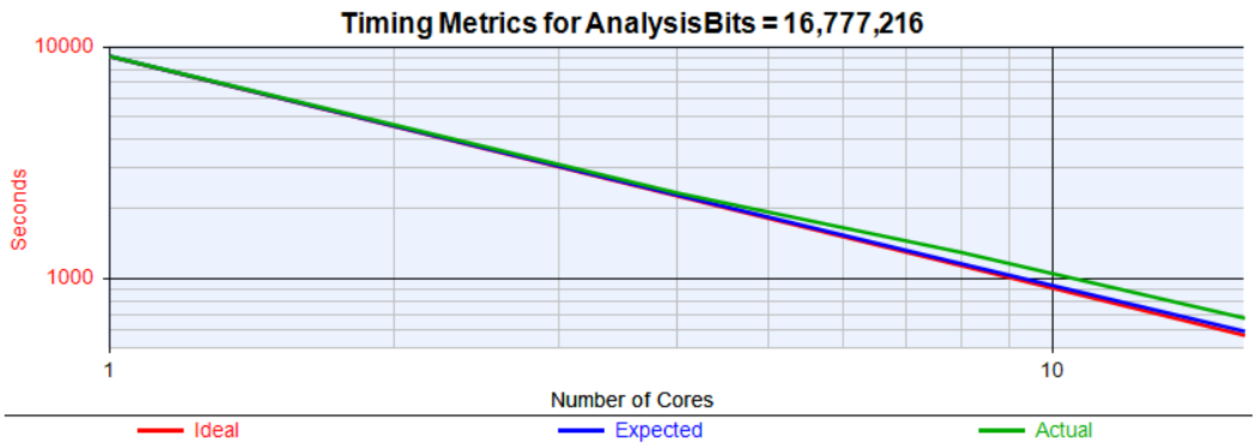
Observation: All BER curves are equally valid. Since it is known that the jitter statistics is different for each simulation, it is understood that the Extrapolated BER curves with have some variation.

<u>AnalysisBits = 16,777,216; NumCores = 1, 2, 4, 8, 16</u>

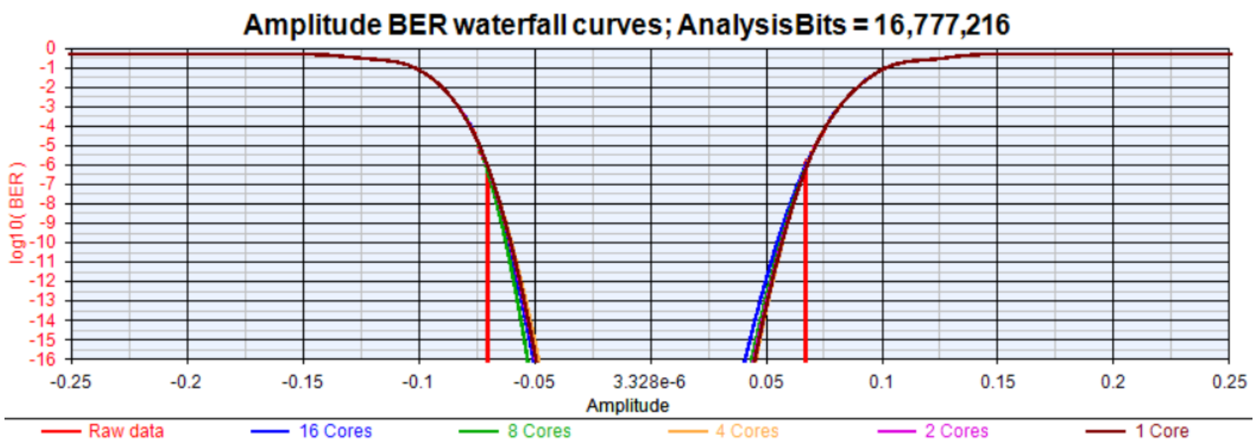
AnalysisBits	16,777,216	Overhead	20.000
#Cores	Ideal	Expected	Actual
1	9439.00	9459.00	9459.00
2	4719.50	4739.50	4740.00
4	2359.75	2379.75	2413.00
8	1179.88	1199.88	1345.00
16	589.94	609.94	731.00

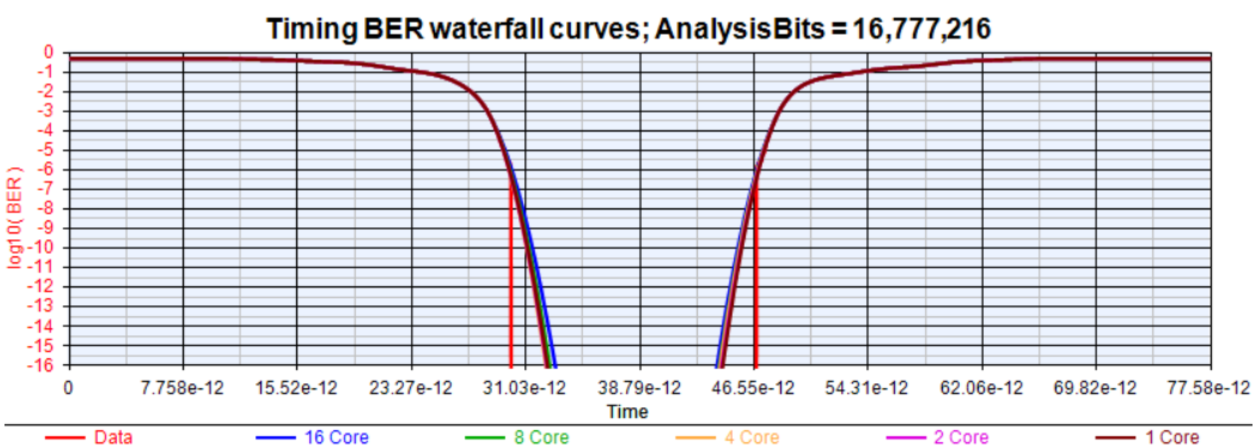
Observation: The actual times increase above the expected times as the number of cores increases. This is as expected for the larger AnalysisBits tests.

This tabular data is shown graphically in this chart with log(time) for the y-axis and log(number of cores) for the x-axis:



Observation: The Ideal curve is a straight line. The Expected curve deviates from the Ideal as a result of the additional constant Overhead_time. The Actual curve deviates from the Expected as Number of Cores increases by an amount that is attributed to the incremental increase in the time for multi-core communication and processing.





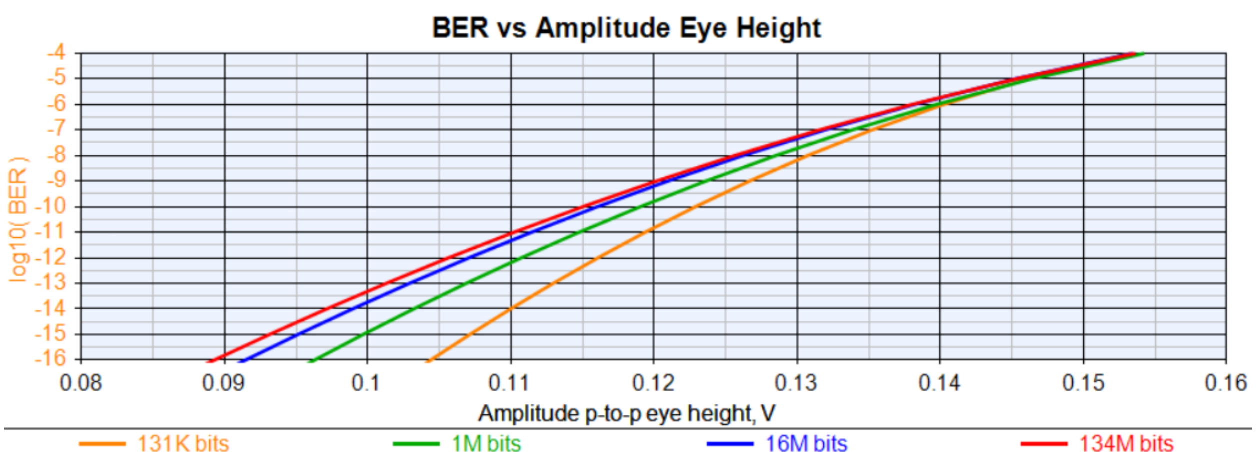
Observation: All BER curves are equally valid. Since it is known that the jitter statistics is different for each simulation, it is understood that the Extrapolated BER curves with have some variation.

Amplitude BER waterfall curve performance for the different AnalysisBits.

The Amplitude BER waterfall curves for the different AnalysisBits are compared by arranging the data to show the BER vs. amplitude eye height. The nominal p-to-p eye height = 0.25 V.

Settings:

- The BER for 131,072 bits is with 2 Cores.
- The BER for 1,048,576 bits is with 4 Cores.
- The BER for 16,777,216 bits is with 16 Cores.
- The BER for 134,217,728 bits is with 28 Cores.
- The BER for 1,073,741,824 bits is with 28 Cores.



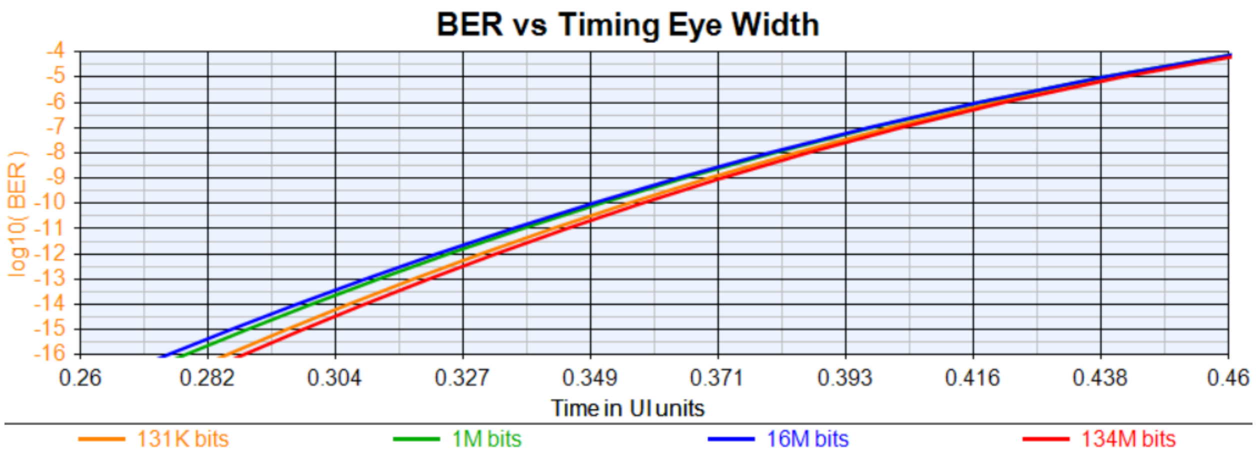
Observation: As can be seen, the amplitude BER eye height decreases as the number of bits increases. The extrapolated BER is more accurate as the AnalysisBits increases. The curves appear to converge to the solution shown for AnalysisBits = 134,217,728. At BER = 10^(-12), the eye height is about 0.106 (42% nominal p-to-p eye height).

Timing BER waterfall curve performance for the different AnalysisBits.

The Timing BER waterfall curves for the different AnalysisBits are compared by arranging the data to show the BER vs. timing eye width. 1 UI is 38.79e-12 sec.

Settings:

- The BER for 131,072 bits is with 2 Cores.
- The BER for 1,048,576 bits is with 4 Cores.
- The BER for 16,777,216 bits is with 16 Cores.
- The BER for 134,217,728 bits is with 28 Cores.
- The BER for 1,073,741,824 bits is with 28 Cores.



Observation: As can be seen, the timing BER eye width varies as the number of bits increases. The extrapolated BER is more accurate as the AnalysisBits increases. The curves appear to converge to the solution shown for AnalysisBits = 134,217,728. At BER = 10^(-12), the eye width is about 0.33 UI (12.8 psec).

Conclusion for The Run Time Metrics with Tx Timing Jitter

The above Channel Simulation tests with NRZ data show that with Tx Timing Jitter, the simulation results with various AnalysisBits and various number of Cores used produce meaningful results.

Due to the random number generator used in generating the Tx timing jitter, the BER results vary with each simulation run. For a constant AnalysisBits, the BER results obtained for various number of Cores used are consistently clustered together.

The BER results are considered to be more accurate as the AnalysisBits increases. The simulation time, compared to the time with the use of 1 Core, can be substantially decreased as the number of Cores are used; 3.5x with 4 Cores; 7x with 8 Cores; 13x with 16 Cores, 23x with 28 Cores.

Thus, one can obtain more accuracy with larger AnalysisBits with less simulation time with no compromise in the analysis results accuracy when using multiple Cores.