Subject: Extracting Modeling Data for a Rx CTLE Circuit

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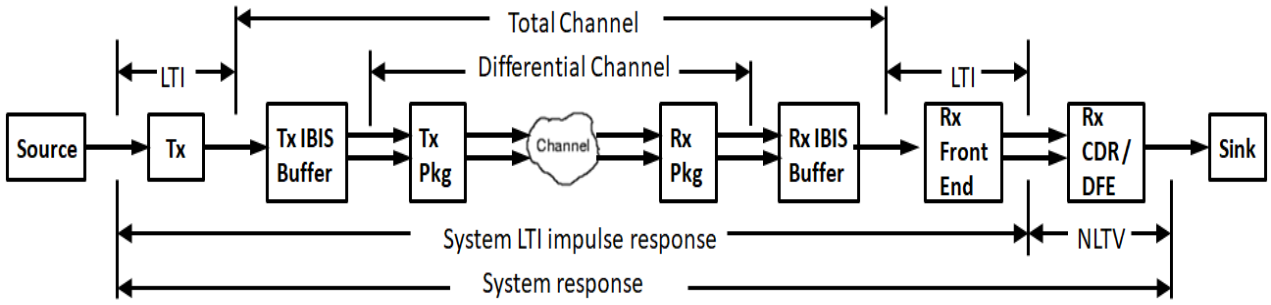
This document discusses features on the web site: **https://www.serdesdesign.com**

A SerDes system for a single channel has the typical structure shown in this figure.

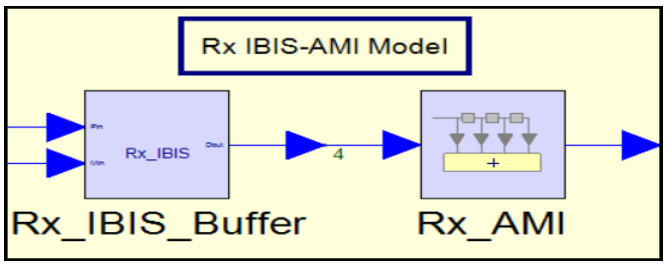


See details in **About the SerDes System Single Channel Tool...**

This document discusses the approach used to extract modeling data for a receiver (Rx) circuit that is a continuous time linear equalizer (CTLE) typically located in the Rx Front End.

Rx IBIS-AMI Model

The Rx circuit is to be modeled as a Rx IBIS-AMI model per the IBIS-AMI standard. The Rx IBIS-AMI model has an IBIS portion and an AMI portion as shown here.



Conceptually, the Rx_IBIS portion takes an input differential signal and outputs a single ended signal. The Rx AMI model receives that single ended signal and outputs a modified single ended signal.

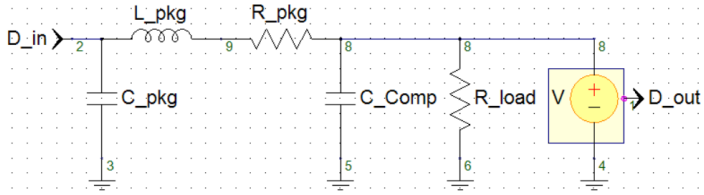
The Rx IBIS-AMI model is typically defined as linear and time invariant (LTI), but may be defined as nonlinear and/or time variant (NLTV) if it contains any nonlinearities. Besides the CTLE, the Rx circuit may also contain a clock and data recovery (CDR) circuit or a decision feedback equalizer (DFE). Such a CDR and DFE are not discussed in this paper.

When the Channel Simulator is run (in its Statistical mode or Bit-by-Bit mode), one input to the Rx_AMI portion from the Channel Simulator is the single ended impulse response that represents the total channel preceding the Rx AMI model and is inclusive of the Rx IBIS characteristic.

Rx IBIS input buffer definition

The Rx model has an associated *.ibs file representing the Rx model IBIS analog input buffer characteristic.

Within the Rx IBIS buffer, the circuit associated with the positive path (P) and the minus path (M) has this circuit representation for each differential input pin:



Where D_out (P) - D_out (M) is the input for the AMI section.

R_load is defined by the *.ibs file [GND Clamp] and [Power Clamp] V-I tables and the other circuit elements are also defined in the *.ibs file.

The V-I tables [GND Clamp] and [Power Clamp] can represent a nonlinear impedance, but for use with a Channel Simulator it is recommended that these tables represent a linear resistance. The reason is that any nonlinearity in the *.ibs file is not used by the Channel Simulator. Instead, the Channel Simulator replaces any nonlinearity with a linear resistance that it decides is appropriate (but typically does not tell the user what it selected). Therefore, defining the linear resistance eliminates the uncertainty (and unpredictability) on the Channel Simulator linearization process. Typically [GND Clamp] is used to represent R_load and [Power Clamp] is set to a high impedance.

Typically, R_load is associated with [GND Clamp] and [Power Clamp] is set to a high resistance.

R_pkg, L_pkg, C_pkg, C_comp and R_load and may have different values for corner cases Typical, Min and Max.

See more detail on the Rx IBIS buffer definition at this link:
https://www.serdesdesign.com/home/web_documents/models/Rx_IBIS_Buffers_used_in_SerDes_Simulations.pdf

RX AMI Modeling Assumptions

The CTLE is assumed to be modeled with a linear and time invariant (LTI) equalizer (F1) with a possible nonlinearity (NL1).

The CTLE circuit is to be treated as a block box and only input and/or output data can be collected.

The objective is to convert the circuit data into an Rx CTLE model.

F1 and NL1 change as the CTLE settings change and will be obtained by extractions from waveforms for each corner case.

For discussion purposes, assume the possible CTLE states for the Rx circuit is 16.

Rx AMI Small Signal Modeling Approach 1

This modeling approach relies on time domain data.

The Rx circuit is to be treated as a black box with Spice circuit time domain simulation stimulus/response waveforms captured for each of the three corner cases from which the circuit model can be extracted.

The modeling approach is based on these steps.

- Operate the CTLE in its small signal region to collect F1 modeling data.
- Record waveforms while varying the CTLE over its full range of settings.
    - Use a data pattern that repeats N 0's, N 1's where N is selected to be long enough to capture the step transient, but not longer.
    - Do this only at the highest bit rate and assume the results apply for all bit rates.
    - Use a maximum time step that is 1/32 * the bit time associated with the highest bit rate.
    - This means for the 3 corner cases there are 16 * 3 = **48 waveform simulations**.
    - This data is used to get the CTLE F1 filtering characteristics.

Rx AMI Small Signal Modeling Approach 2

This modeling approach relies on frequency domain data.

The Rx circuit is to be treated as a black box with Spice circuit AC simulation frequency domain data captured for each of the three corner cases from which the circuit model can be extracted.

The modeling approach is based on these steps.

- Operate the CTLE in its small signal region to collect F1 modeling data.
- Record frequency domain data while varying the CTLE over its full range of settings.
    - Be sure to set the frequency step small enough and the maximum frequency high enough to retain the fidelity of the circuit.
    - The frequency sweep should be linear with the frequency step.
    - This means for the 3 corner cases there are 16 * 3 = **48 AC simulations**.
    - This data is used to get the CTLE F1 filtering characteristics.

Rx AMI Nonlinearity Modeling Approach

There are many ways for modeling a nonlinearity.

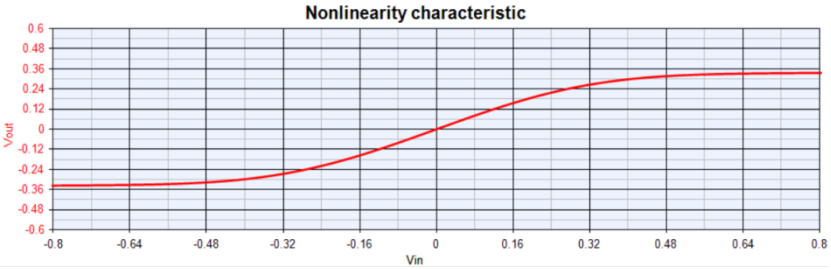
For this modeling purpose, it is assumed that the circuit nonlinearity can be effectively defined as a memory-less nonlinearity that is cascaded after the F1 filter and that the nonlinearity can be defined using Spice circuit simulation to collect the DC vout vs vin characteristic where vin is swept over its nonlinear region of interest.

This data is collected while varying the CTLE over its full range of settings for each of three corner cases.

This means for the 3 corner cases there are 16 * 3 = **48 Swept DC simulations**.

This data inherently includes the CTLE small signal gain which will be removed when using this NL1 data with the F1 data.

Here is what a typical nonlinearity curve would look like.



Option to De-Embed the IBIS Characteristic from the Rx AMI Model

For each Rx AMI modeling approach, the Rx AMI model can be obtained from the Rx circuit data directly if the response did not include the IBIS buffer characteristic or, at the customer option, the characteristics of the IBIS buffer can be de-embedded from the circuit response data if the waveform response did include the IBIS buffer characteristic.

For the de-embedding option, the Rx IBIS buffer impulse characteristic is de-embedded from the Rx response data to obtain the Rx AMI characteristics. Together, the Rx AMI and Rx IBIS buffer characteristics will achieve the Rx responses provided by the customer.

Waveform Time Domain File Format

Typically, one Rx circuit stimulus waveform is associated with a set 'M' of Rx circuit response waveforms.

One stimulus waveform data file has one associated response waveform data file containing M responses.

As discussed in the next section, the waveform response data is collected for all M states of the circuit and placed into a text file as comma separated variables (*.csv).

If the time values for all M waveform responses are the same, then the response waveform file would have 1+M columns where the first column is for time values followed by M columns for the response waveform values.

If the time values for all M response waveforms are not the same, then file would have 2*M columns where each pair of consecutive columns are for the time and voltage pairs for each waveform response. In this case, if the waveform responses do not have the same number of data points, then fill in their columns with -1 for their time and voltage pairs for their remaining rows up to the maximum number of rows associated with the longest response.

Spectrum Frequency Domain File Format

Typically one file is ssociated with a set 'M' of Rx spectrum response.

The AC spectrum data is collected for all M states of the circuit and placed into a text file as comma separated variables (*.csv).

If the frequency values for all M spectrums are the same, then the file would have 1+2*M columns where the first column is for frequency values followed by 2 columns (magnitude, phase) for each of the M spectrums.

If the frequency values for all M spectrums are not the same, then file would have 2*2*M columns where each triplet of consecutive columns are for the frequency, magnitude and phase for each spectrum. In this case, if the spectrums do not have the same number of data points, then fill in their columns with -1 for their frequency, magnitude and phase triplets for their remaining rows up to the maximum number of rows associated with the longest spectrum.

Typical process for collecting time domain waveform stimulus and response data

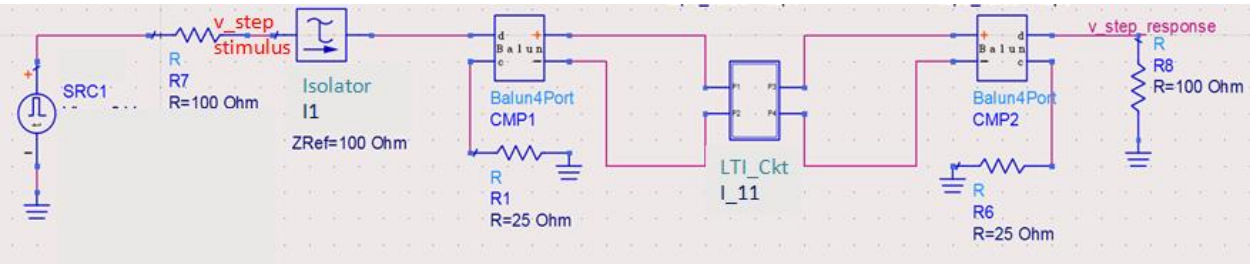
One circuit may have various states, each of which needs to be characterized with its waveform response. Let the number of circuit operating states be represented with the variable M. In this example test case let M = 10

The following discusses a typical process for collecting step response data using the Keysight Advanced Design System (ADS) transient circuit simulator. A similar process can be defined for any other transient circuit simulator. Though the CUSTOMER owns the procedure for setup and simulation, the typical process will be similar to the ADS transient setup and simulation discussed here.

A typical ADS workspace contains schematics and data displays. Here, one is shown with a circuit schematic and data display.

It is used to demonstrate setup and collection of the circuit waveforms. Though there are many ways of doing this, the current demonstration is just one way that can be generalized and adapted for collecting the circuit waveforms in other ways.

The circuit that is to be evaluated is operating at a 8 Gbps bit rate. The details of the circuit are not shown. Only the top level circuit simulation design is shown.



Not shown in this schematic are the ADS Tran (transient) simulation controller, VAR (variable) blocks, MeasEqn (measurement equation) blocks, ParamSweep (parameter sweep) block and any other assorted block needed for running the simulation.

The circuit has differential loading at its input and output (100 ohm differential loading).

Note: If the Rx IBIS model has R_load different from 50 ohms (see topic 'Rx IBIS output buffer definition' above), then set R7 = 2*R_load and R1 = R_load/2.0.

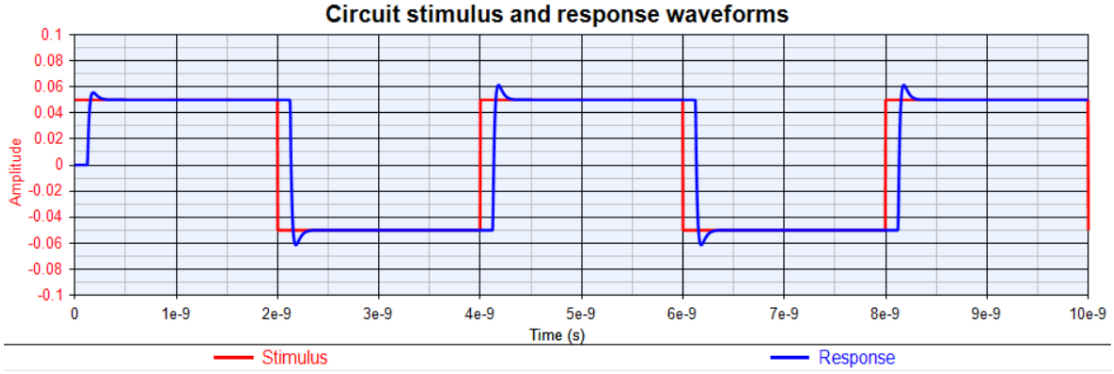
The single ended waveform stimulus is converted to a differential waveform stimulus using a Balun4Port. The output differential waveform response is converted to a single ended waveform response using a Balun4Port as well. The input waveform stimulus value has the named node v_step_stimulus. Note that the isolator eliminates the effects of the circuit input reflections from the recorded stimulus so that the stimulus has sharp and unambiguous transition times. The output waveform response value has the named node v_step_response. The single ended waveform response is really what is needed for the AMI modeling. There is no need to export the positive and negative sides of the differential waveform response separately, but that can be done if preferred by CUSTOMER.

This Tran circuit simulation controller is set up with StopTime = 10 nsec (enough time for 80 bit UIs which in this example is considered long enough to capture multiple waveform cycles), and MaxTimeStep = 3.90625 psec (which is 1 UI divided by 32 since the Channel Simulation will use 32 samples per UI). The StopTime should be at least 2X time the circuit start up transient.

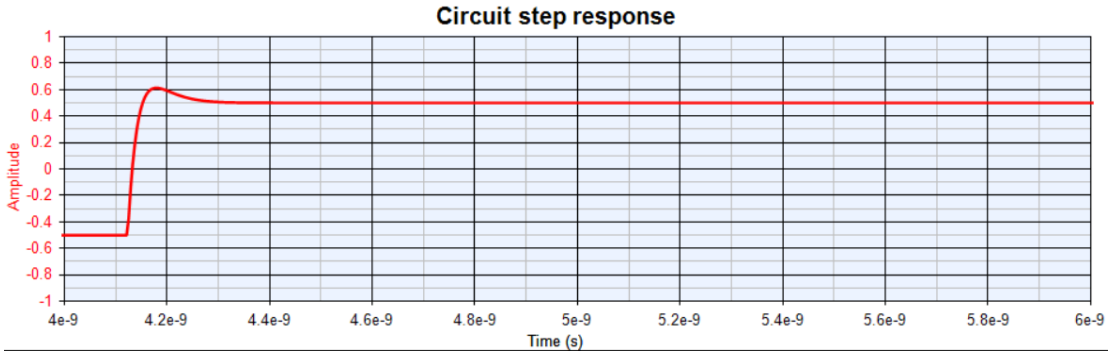
The source (SRC1) is actually a bit pattern waveform generator with a repeating pattern of N 1's and N 0's where N is long enough to capture the step transitions of the FFE circuit. In this test case N = 16. The waveform generator is achieved with settings for Vlow = 0, Vhigh = 2*InputStepStimulus, Rise and Fall times set to 1 UI/32. InputStepStimulus is set to a level that operates the circuit in its linear region. In this test case, InputStepStimulus = 0.25.

With the circuit set up at one of its M operating states, the circuit simulation is run and the stimulus and response waveforms are observed.

Circuit stimulus and response waveforms.



The step response to be captured is after the initial start up transient. In this case, the response waveform from 4.0e-9 sec to 5.9e-9 sec will be captured and used as the step response which is shown here:



Only this portion of the response waveform should be captured to represent the circuit step response.