Subject: Extracting Modeling Data for a Tx FFE Circuit

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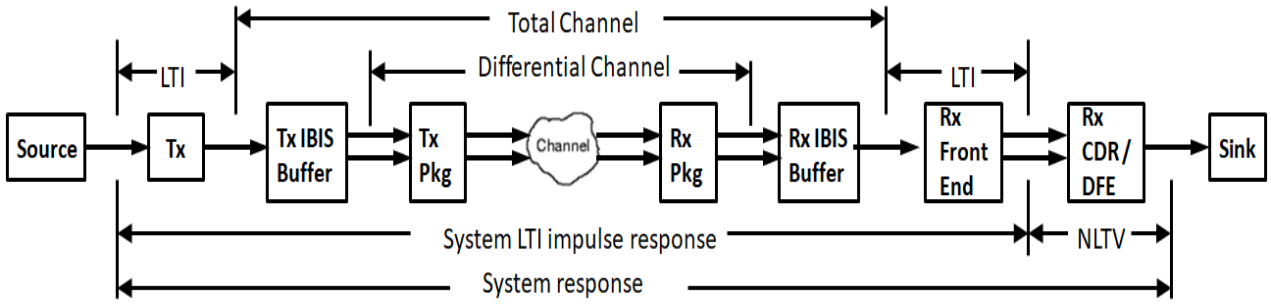
This document discusses features on the web site: **https://www.serdesdesign.com**

A SerDes system for a single channel has the typical structure shown in this figure.

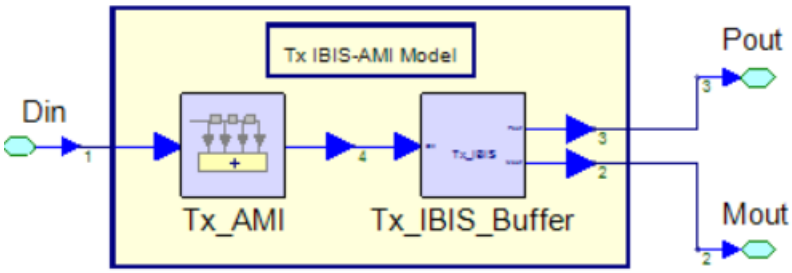


See details in **About the SerDes System Single Channel Tool...**

This document discusses approaches used to extract modeling data for a transmit (Tx) circuit that is a feed forward equalizer (FFE).

Tx IBIS-AMI Model

The Tx circuit is to be modeled as a Tx IBIS-AMI model per the IBIS-AMI standard. The Tx IBIS-AMI model has an AMI portion and an IBIS portion as shown here.



Conceptually, the Tx_AMI portion takes an input single ended NRZ data stream and outputs a filtered NRZ singled ended data stream. The Tx IBIS Buffer receives that single ended signal and outputs a differential signal to be connected to a differential channel.

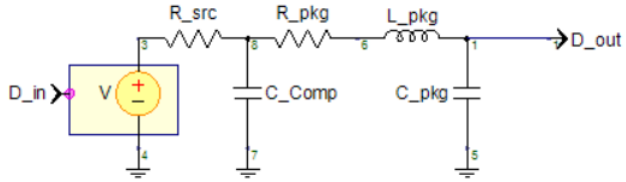
This Tx IBIS-AMI model is defined as linear and time invariant (LTI). In practice, when the Channel Simulator is run (in its Statistical mode or Bit-by-Bit mode), the Tx_AMI portion input from the Channel Simulator is a single ended impulse response and it outputs is a modified single ended impulse response.

The Tx IBIS Buffer characteristic is included by the Channel Simulator into the total single ended impulse response for the channel between the Tx_AMI and Rx_AMI models.

The Tx circuit to be modeled is a feed forward equalizer (FFE) model and may be linear or nonlinear. Even if the FFE circuit is nonlinear, the modeling approach discussed in this paper is still valid in representing the circuit as a Tx IBIS-AMI LTI model.

Tx IBIS output buffer definition

The Tx model has an associated *.ibs file representing the Tx model IBIS analog output buffer characteristic. Within the Tx IBIS buffer, the circuit associated with the positive path (P) and the minus path (M) has this circuit representation for each differential output pin:



Where D_in is the input from the AMI section. The circuit is the same for the P and M paths and D_out represents the P or M output.

R_src is defined by the *.ibs file [Pulldown] and [Pullup] V-I tables and the other circuit elements are also defined in the *.ibs file.

The V-I tables [Pulldown] and [Pullup] can represent a nonlinear impedance, but for use with a Channel Simulator it is recommended that these tables represent a linear resistance. The reason is that any nonlinearity in the *.ibs file is not used by the Channel Simulator. Instead, the Channel Simulator replaces any nonlinearity with a linear resistance that it decides is appropriate (but typically does not tell the user what it selected). Therefore, defining the linear resistance eliminates the uncertainty (and unpredictability) on the Channel Simulator linearization process.

These values can be defined as part of the circuit characteristics:

R_pkg, L_pkg, C_pkg, C_comp and R_src and may have different values for corner cases Typical, Min and Max.

Note on the use of C_Comp in a Tx IBIS model

Due to the IBIS-AMI standard, a non-zero C_comp value may have a conflict with the [Ramp] section used in the Tx IBIS Buffer for a Tx IBIS-AMI model.

Here is a quote from the IBIS standard for the [Ramp] section.

Keyword: **[Ramp]**

Required: Yes, except for inputs, terminators, Series, and Series_switch model types

Description: Defines the rise and fall times of a buffer. The ramp rate does not include packaging but does include the effects of the C_comp or C_comp_* parameters.

In other words, for a Tx IBIS-AMI model [Ramp] is required AND when used is to include the effects of C_comp which should be set to zero.

However, one can include non-zero C_comp values if in the [Ramp] section one sets the rise and fall times to a very fast value such that it does not duplicate the effects of C_comp.

Alternative to the Tx IBIS output buffer

In many cases, the simplified circuit permitted by the IBIS-AMI standard for use as the Tx IBIS output buffer is not adequate for a customer needs.

An alternative is to take one of these two approaches. Both approaches require supplementing the IBIS-AMI model with a separate 4 port S-Parameter file.

Alternative 1: This alternative is compliant with the IBIS-AMI standard.

- In the *.ibs file, define the Tx IBIS output buffer to be ideal by setting R_pkg = L_pkg = C_pkg = C_comp = 0, and R_src = 50 Ohms (or whatever is desired).
- Use an external 4 port (differential in and out) S-Parameter file that defines the actual impedance characteristic one would like to use in place of the Tx IBIS buffer.

Alternative 2: This alternative is supported based on the IBIS 7.0 standard, not earlier.

- Tx IBIS output buffer can be somewhat arbitrary except for the [Algorithmic Model] lines since the Tx IBIS buffer will not be used.
- Instead, place these lines in the *.ami file under Model_Specific parameters:

(Tx_V (Usage Info) (Value 1.0) (Type Float) (Description "Output open circuit high voltage"))

(Tx_R (Usage Info) (Value 0.0) (Type Float) (Description "Driver series resistance"))

(Tstonefile (Usage Info) (Type String) (Value "driver.s4p") (Description "On-die S-parameters"))

- When used in ADS, these *,ami file lines will replace the IBIS buffer in the *.ibs file with this S-parameter file.

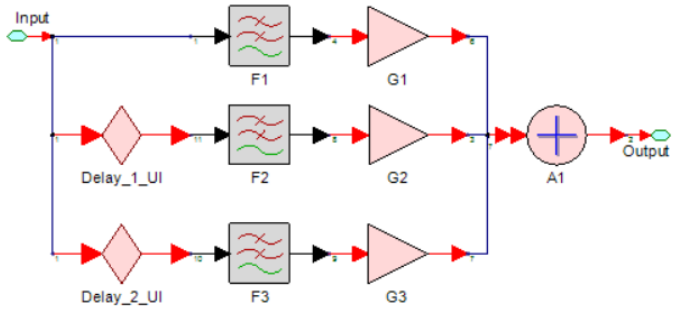
Both of the above alternatives require that the S-parameter file be delivered with the IBIS-AMI model.

TX AMI Modeling Assumptions

For discussion purpose, this Tx FFE example is assumed to have one pre-cursor and one-post cursor. For general purpose, the FFE can have any number or pre and post cursors.

The FFE circuit is to be treated as a block box and only time domain input and output waveform data can be collected.

The FFE essentially has this equivalent block diagram:



The objective is to convert the circuit input and output waveform data into the Tx FFE model.

G1, G2, G3 are gain block whose gain changes as the settings for the FFE tap settings changes and these gain value cannot be defined on their own. G1 is the pre-cursor gain setting. G2 is the main cursor gain setting. G3 is the post-cursor gain setting. These gain values are unknown.

F1, F2 and F3 are linear time invariant (LTI) filters and these filters cannot be characterized on their own. Assume all of these filters have zero DC gain. These filtering functions are unknown and can be dependent on the G values.

The filter characteristics and gain values will be obtained by extractions from waveforms for each corner case.

Assume one need only collect data using negative values for the pre-cursor and post-cursor and that any response with positive pre-cursor or post-cursor settings are just the inverse of that obtain with these positive settings.

Typically the main tap gain G2 is derived from the pre and post-cursor gains (G1 and G3) and the output amplitude where the output amplitude corresponds with zero pre and post cursor gain settings.

For discussion purposes, assume these possible states for the Tx circuit:

- Number of pre-cursor settings: 13
- Number of post-cursor tap settings: 17
- Number of amplitude settings: 14

Tx AMI Modeling Approach 1

This modeling approach is the most detailed.

The Tx circuit is to be treated as a black box with Spice circuit time domain simulation stimulus/response waveforms captured for each of three corner cases from which the circuit model will be extracted.

The modeling approach is based on these steps.

- Record waveforms while varying the pre-cursor, post-cursor and amplitude over their full range of settings.
    - Use a data pattern that repeats N 0's, N 1's where N is selected to be long enough to capture the step transient, but not longer.
    - Do this only at or below the lowest bit rate and assume the results apply for all bit rates.
        - Be sure that the bit rate is small enough to ensure settling for during the pre-cursor and post-cursor time intervals.
    - Use a maximum time step that is 1/32 * the bit time associated with the largest bit rate.
    - This means for the 3 corner cases there are 13 * 17 * 14 * 3 = **9,282 waveform simulations**.
    - This data is used to get the FFE tap values and FFE filtering characteristic

- Assume one need only collect data using negative values for the pre-cursor and post-cursor.
    - Assume any response with positive pre-cursor or post-cursor settings are just the inverse of that obtain with these negative settings.

This modeling approach can result in set of waveform simulation that is too large from a practical data collection point of view. It can be realistic when the number of states for the pre-cursor, post-cursor and amplitude is reduced. For example, these states are 4, 4 and 4, then the total number of waveform simulation is 64 which may be practical.

Tx AMI Modeling Approach 2

This modeling approach still captures a lot of detail, but uses simplifying assumptions.

The Tx circuit is to be treated as a black box with Spice circuit time domain simulation stimulus/response waveforms captured for each of three corner cases from which the circuit model will be extracted.

The modeling approach is based on these steps.

- Record waveforms while varying amplitude over its full range set with the pre-cursor and post-cursor tap values set to zero.
    - Use a data pattern that repeats N 0's, N 1's where N is selected to be long enough to capture the step transient, but not longer.
    - Do this only at or below the lowest bit rate and assume the results apply for all bit rates.

    - Be sure that the bit rate is small enough to ensure settling for during the pre-cursor and post-cursor time intervals.
  - Use a maximum time step that is 1/32 * the bit time associated with the largest bit rate.
  - With 14 possible amplitude settings, this means for the 3 corner cases there are 14 * 3 = **42 waveform simulations**.

- Assume one need only collect data using negative values for the pre-cursor and post-cursor.
  - Assume any response with positive pre-cursor or post-cursor settings are just the inverse of that obtain with these negative settings.

- Record waveforms with pre-cursor varied over its settings and the post-cursor varied over its settings. Set the amplitude for its setting for maximum amplitude.
  - Use a data pattern that repeats N 0's, N 1's where N is selected to be long enough to capture the step transient, but not longer.
  - Assume settings with the amplitude with smaller amplitude settings just requires linear scaling.
  - Do this only at or below the lowest bit rate and assume the results apply for all bit rates.
  - Use a maximum time step that is 1/32 * the bit time associated with the largest bit rate.
  - With 13 possible pre-cursor settings and 17 possible post-cursor settings, this results in 13 * 17 = 221 waveforms for each corner case.
  - For three corner cases, this results in **663 waveform simulations**.
  - This data is used to get the FFE tap values and FFE filtering characteristic

Tx AMI Modeling Approach 3

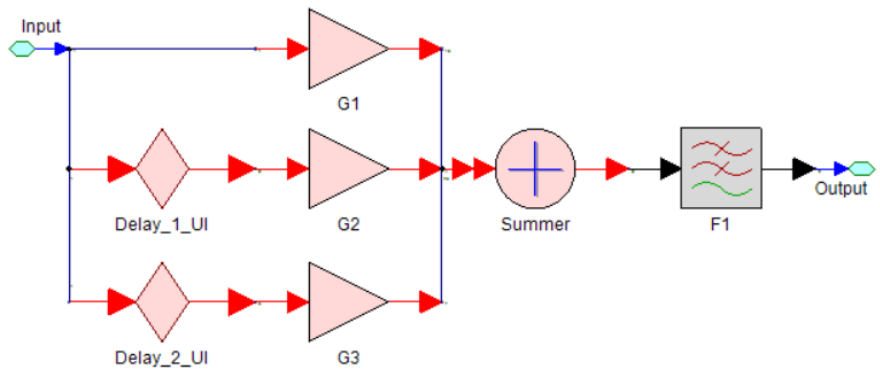
This modeling approach is the least detailed and most often is enough to achieve a high fidelity Tx IBIS-AMI model.

The Tx circuit is to be treated as an FFE with known pre-cursor gain values, known post-cursor gain values, known amplitude values, and a given relationship between these values. The only unknown is the filter (F1) common to all three FFE taps.

For the relationship between pre-cursor, pos-cursor and amplitude value, one common relationship is for the sum of the absolute value of the taps to equal the defined amplitude. Let A = amplitude and G1, G2, G3 represent the pre-cursor gain, main tap gain and post-cursor tap gain respectively. The value of G2 is derived from A, G1 and G3 as follows:

G2 = A - abs(G1) - abs(G3).

See this simplified Tx AMI model block diagram:



The modeling approach is based on capturing waveform responses from Spice circuit simulations. This approach is to be done for each of three corner cases.

- Record waveforms with the pre and post cursor set to zero and by varying the amplitude over its full range of setting.
    - Use a data pattern that repeats N 0's, N 1's where N is selected to be long enough to capture the step transient, but not longer.
    - Do this only at or below the lowest bit rate and assume the results apply for all bit rates.
    - Use a maximum time step that is 1/32 * the bit time associated with the largest bit rate.
    - This means for the 3 corner cases there are 14 * 3 = **42 waveform simulations**.
    - This data is used to get the F1 filtering characteristic

This modeling approach is often enough to achieve a high fidelity Tx IBIS-AMI model.

It is the Tx circuit designers decision as to which Tx IBIS-AMI modeling approach should be used to model their Tx circuit.

Option to De-Embed the IBIS Characteristic from the Tx AMI Model

For each Tx AMI modeling approach, the Tx AMI model can be obtained from the Tx circuit stimulus/response waveform directly if the waveform response did not include the IBIS buffer characteristic or, at the customer option, the characteristics of the IBIS buffer can be de-embedded from the circuit response waveforms if the waveform response did include the IBIS buffer characteristic.

For the de-embedding option, the Tx IBIS buffer impulse characteristic is de-embedded from the Tx waveform response data to obtain the Tx AMI characteristics. Together, the Tx AMI and Tx IBIS buffer characteristics will achieve the Tx waveform responses provided by the customer.

Waveform File Format

Typically one Tx circuit stimulus waveform is associated with a set 'M' of Tx circuit response waveforms. In this case, one stimulus waveform data file has associated M response waveform data files.

As discussed in the next section, the step response data is collected for all M states of the circuit and placed into a text file as comma separated variables (*.csv).

If the time values for all M step responses are the same, then the file would have 1+M columns where the first column is for time values followed by M columns for the step response values.

If the time values for all M step responses are not the same, then file would have 2*M columns where each pair of consecutive columns are for the time and voltage pairs for each step response. In this case, if the step responses do not have the same number of data points, then fill in their columns with -1 for their time and voltage pairs for their remaining rows up to the maximum number of rows associated with the longest response.

Typical process for collecting waveform stimulus and response data

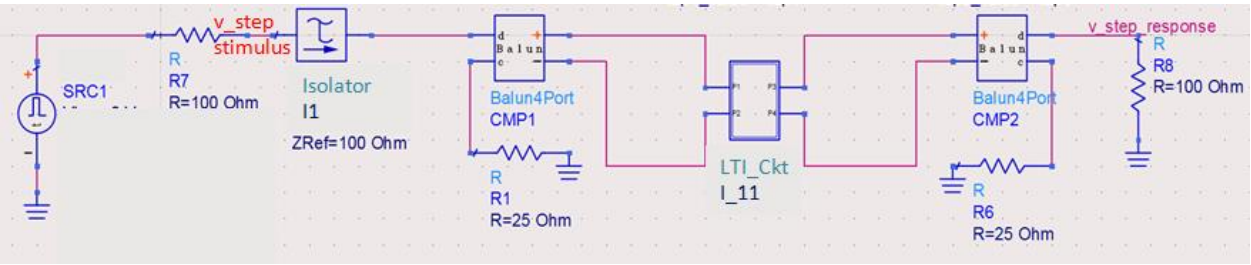
One circuit may have various states, each of which needs to be characterized with its waveform response. Let the number of circuit operating states be represented with the variable M. In this example test case let M = 10

The following discusses a typical process for collecting step response data using the Keysight Advanced Design System (ADS) transient circuit simulator. A similar process can be defined for any other transient circuit simulator. Though the CUSTOMER owns the procedure for setup and simulation, the typical process will be similar to the ADS transient setup and simulation discussed here.

A typical ADS workspace contains schematics and data displays. Here, one is shown with a circuit schematic and data display.

It is used to demonstrate setup and collection of the circuit waveforms. Though there are many ways of doing this, the current demonstration is just one way that can be generalized and adapted for collecting the circuit waveforms in other ways.

The circuit that is to be evaluated is operating at a 8 Gbps bit rate. The details of the circuit are not shown. Only the top level circuit simulation design is shown.



Not shown in this schematic are the ADS Tran (transient) simulation controller, VAR (variable) blocks, MeasEqn (measurement equation) blocks, ParamSweep (parameter sweep) block and any other assorted block needed for running the simulation.

The circuit has differential loading at its input and output (100 ohm differential loading).

Note: If the Tx IBIS model has R_src different from 50 ohms (see topic 'Tx IBIS output buffer definition' above), then set R8 = 2*R_src and R6 = R_src/2.0.

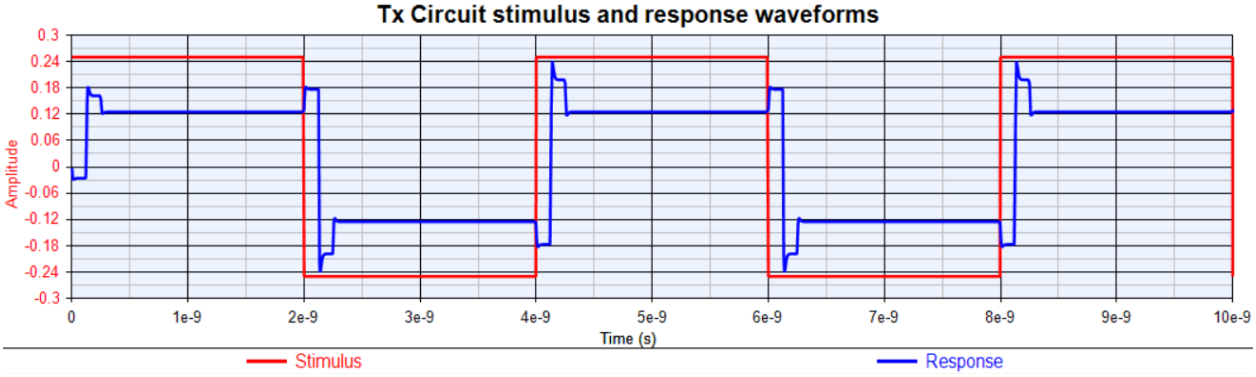
The single ended waveform stimulus is converted to a differential waveform stimulus using a Balun4Port. The output differential waveform response is converted to a single ended waveform response using a Balun4Port as well. The input waveform stimulus value has the named node v_step_stimulus. Note that the isolator eliminates the effects of the circuit input reflections from the recorded stimulus so that the stimulus has sharp and unambiguous transition times. The output waveform response value has the named node v_step_response. The single ended waveform response is really what is needed for the AMI modeling. There is no need to export the positive and negative sides of the differential waveform response separately, but that can be done if preferred by CUSTOMER.

This Tran circuit simulation controller is set up with StopTime = 10 nsec (enough time for 80 bit UIs which in this example is considered long enough to capture multiple waveform cycles), and MaxTimeStep = 3.90625 psec (which is 1 UI divided by 32 since the Channel Simulation will use 32 samples per UI). The StopTime should be at least 2X time the circuit start up transient.

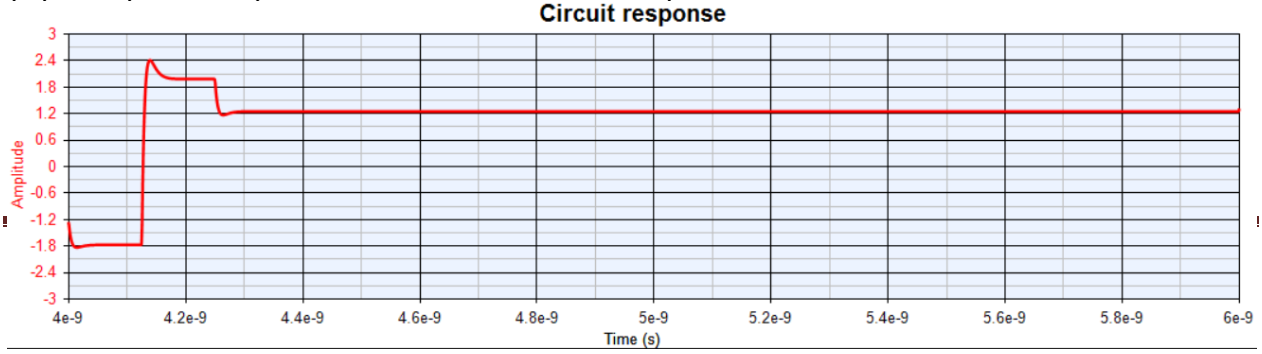
The source (SRC1) is actually a bit pattern waveform generator with a repeating pattern of N 1's and N 0's where N is long enough to capture the step transitions of the FFE circuit. In this test case N = 16. The waveform generator is achieved with settings for Vlow = 0, Vhigh = 2*InputStepStimulus, Rise and Fall times set to 1 UI/32. InputStepStimulus is set to a level that operates the circuit in its linear region. In this test case, InputStepStimulus = 0.25.

With the circuit set up at one of its M operating states, the circuit simulation is run and the stimulus and response waveforms are observed.

Circuit stimulus and response waveforms with non-zero pre-cursor and post-cursor.

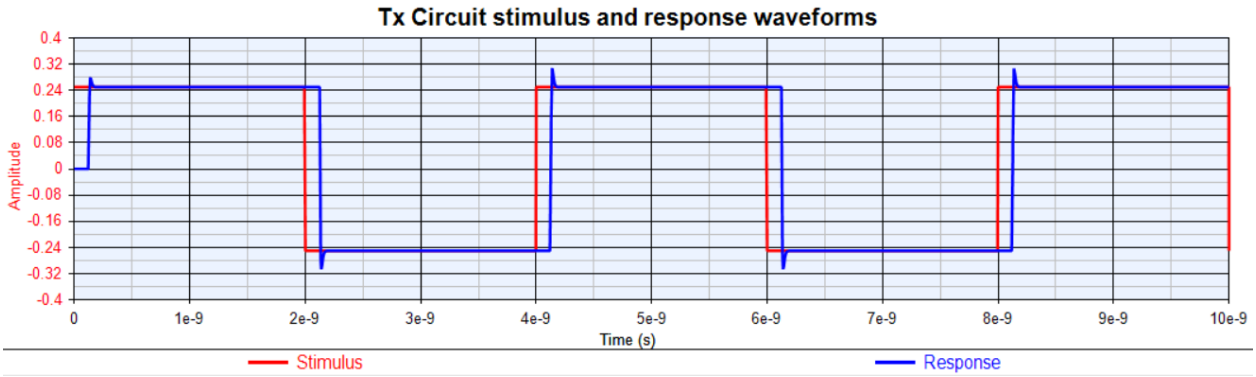


The waveform response to be captured is after the initial start up transient. In this case, the response waveform from 4.0e-9 sec to 5.9e-9 sec will be captured and normalized by 0.25 (InputStepStimulus) and used as the waveform response which is shown here:

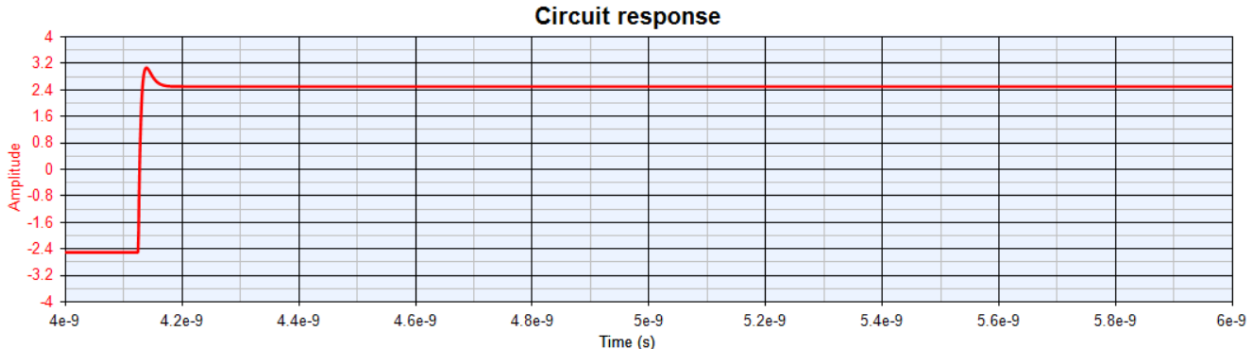


Observe that the pre-cursor and post-cursor response settles within 1 UI.

Circuit stimulus and response waveforms with zero pre-cursor and post-cursor.



The step response to be captures is after the initial start up transient. In this case, the response waveform from 4.0e-9 sec to 5.9e-9 sec will be captured and normalized by 0.25 (InputStepStimulus) and used as the step response which is shown here:



Observe that there is a delay in the response relative to the stimulus.