SerDesDesign.com IBIS-AMI Overview 2020/06/09

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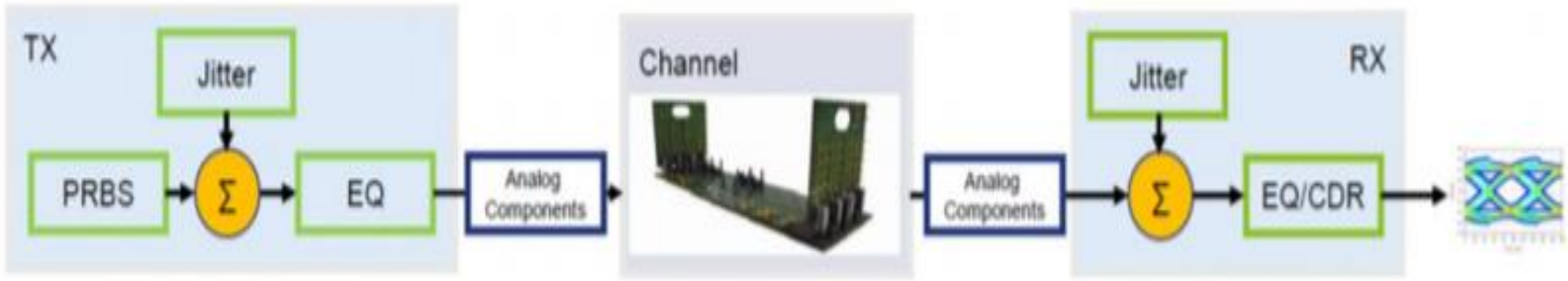
What are IBIS-AMI models?

- IBIS-AMI models were introduced by the IBIS Open Forum (www.ibis.org) with their IBIS 5.0 specification to address the modeling needs for SerDes systems. Today, the IBIS-AMI specification is at revision 7.0.

- IBISver5.0; IBIS version 5.0 ratified August 2008
- IBISver5.1; IBIS version 5.1 ratified 24 August 2012
- IBISver6.0; IBIS version 6.0 ratified 20 September 2013
- IBISver6.1; IBIS version 6.1 ratified 11 September 2015
- IBISver7.0; IBIS version 7.0 ratified 15 March 2019

IBIS-AMI models are used in modeling SerDes systems

- A SerDes (Serializer-Deserializer) is a pair of Tx/Rx blocks used in high speed communications to compensate for lossy channel links to maintain an open eye at the receiver data slicer.
  - PCI Express, HDMI, USB and other types of links.
- Provides serial data transmission typically over a differential pair
  - Multiple SerDes can be used in parallel for higher throughput.
- At higher data rates (>5 Gbps), equalization was introduced with digital signal processing (DSP).
- Analog and DSP functionality is combined into IBIS-AMI models.



Example SerDes

- A Cadence® 112Gbps Multi-Rate PAM-4 SerDes IP
- 7nm semiconductor process technology
- Evaluated by a Keysight Infiniium DCA-X Oscilloscope.

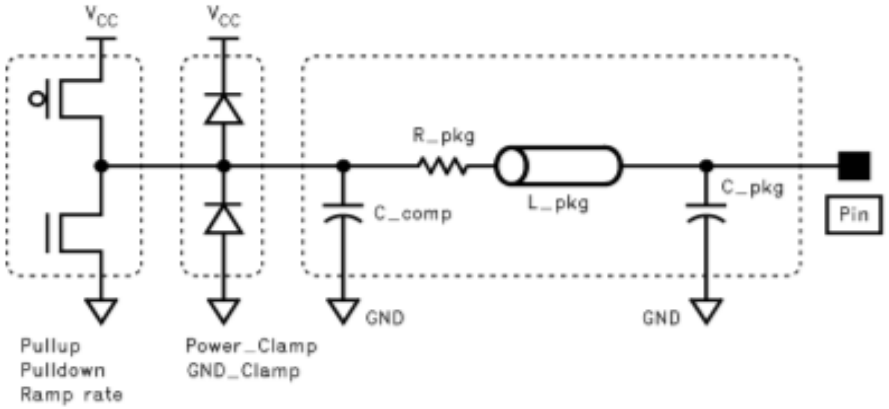
IBIS-AMI is a standard

- IBIS stands for Input/output Buffer Information Specification.
- IBIS-AMI models provide a standardized model interface used by the SerDes chip designers and SerDes system designers.
- The IBIS portion are behavioral models of analog buffers.
- Analog buffers define the SerDes chip impedance interfacing the transmission media.

- Interoperable: different vendor models work together
- Portable: one model runs in multiple simulators
- Flexible: support statistical and time-domain simulation
- High Performance: simulate a million bits per CPU minute
- Accurate: high correlation to simulations / measurement
- Secure: represent IP behavior without exposing internal details

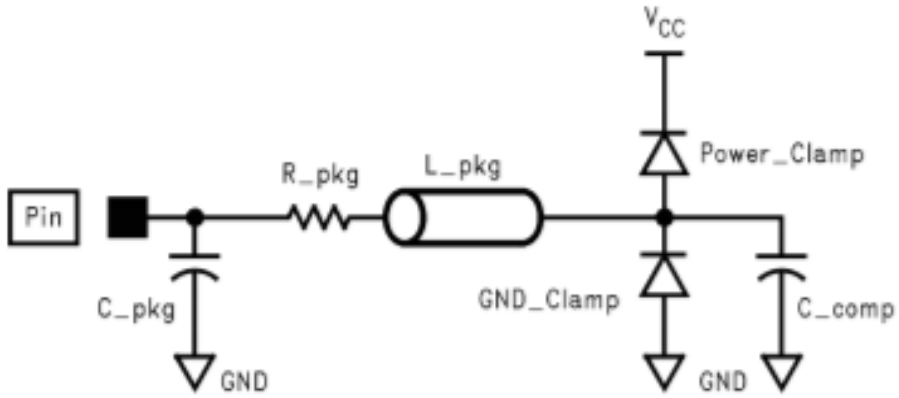
Tx IBIS models

- A Tx IBIS analog output buffer circuit has this simplified representation per pin for a differential output.
- For IBIS-AMI applications only a subset of the IBIS buffer models defined in the IBIS standard are allowed.
- Per the 7.0 standard, it can be defined with an S4P file.



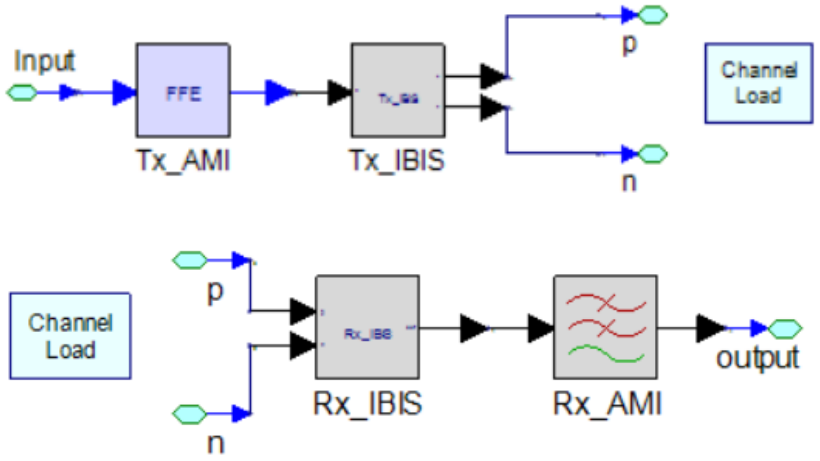
Rx IBIS models

- An Rx IBIS analog input buffer circuit has this simplified representation per pin for a differential input.
- For IBIS-AMI applications only a subset of the IBIS buffer models defined in the IBIS standard are allowed.
- Per the 7.0 standard, it can be defined with an S4P file.



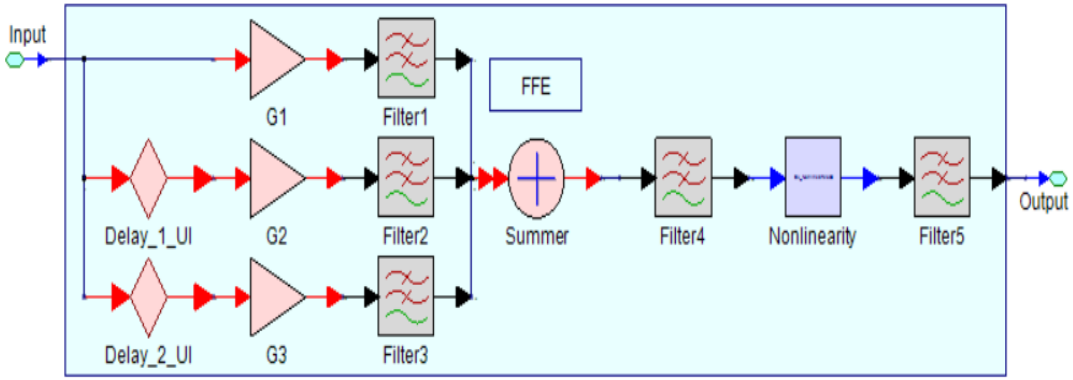
AMI models

- AMI stands for Algorithmic Modeling Interface
- Designed to handle modeling of the signal processing (analog and/or digital) of the SerDes chip.
- The AMI portion can be defined either as linear and time invariant (LTI) or nonlinear and/or time variant (NLTV).



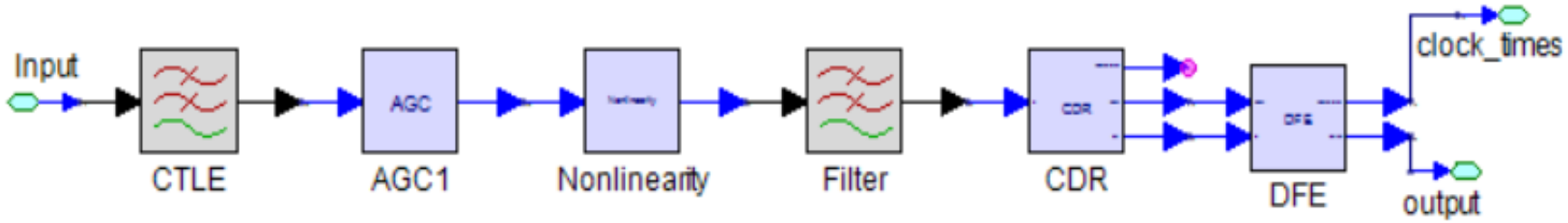
Tx AMI models

- The Tx AMI portion often is a Feed Forward Equalizer (FFE).
- The signal flow graph shown here is for a 3 tap FFE.



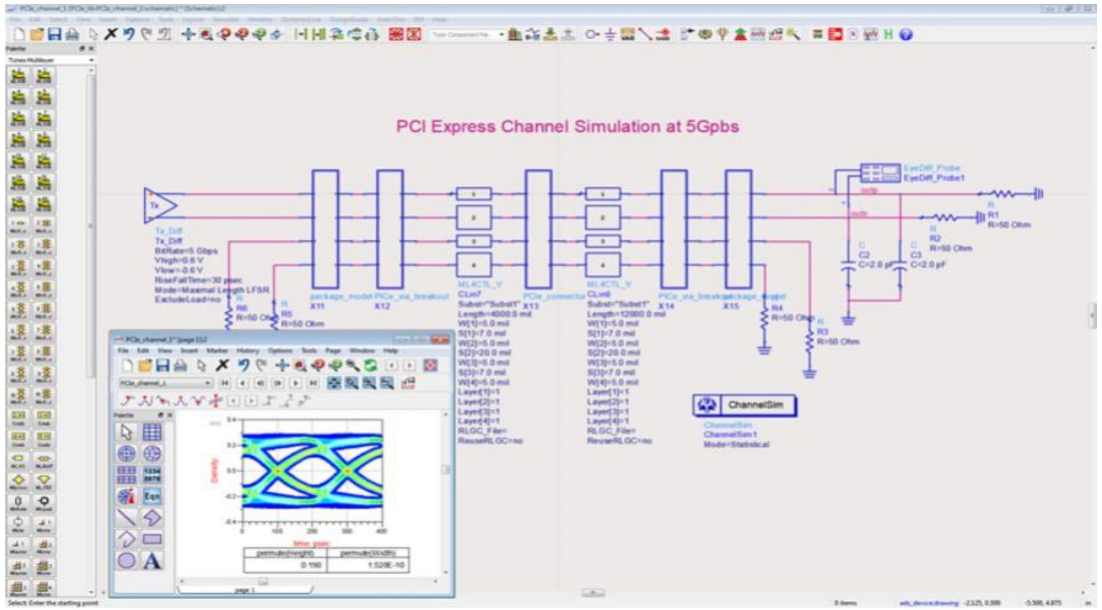
Rx AMI models

- The Rx AMI portion often contains
  - Continuous Time Linear Equalizer (CTLE),
  - Clock and Data Recovery (CDR) circuit and a
  - Decision Feedback Equalizer (DFE)
- The signal flow as shown here is typical.



Using IBIS-AMI models in a Channel Simulator

- Along with the introduction of IBIS-AMI models, a new class of simulator was introduced called a SerDes Channel Simulator.
- Here is a screen capture from the Keysight ADS Channel Simulator.

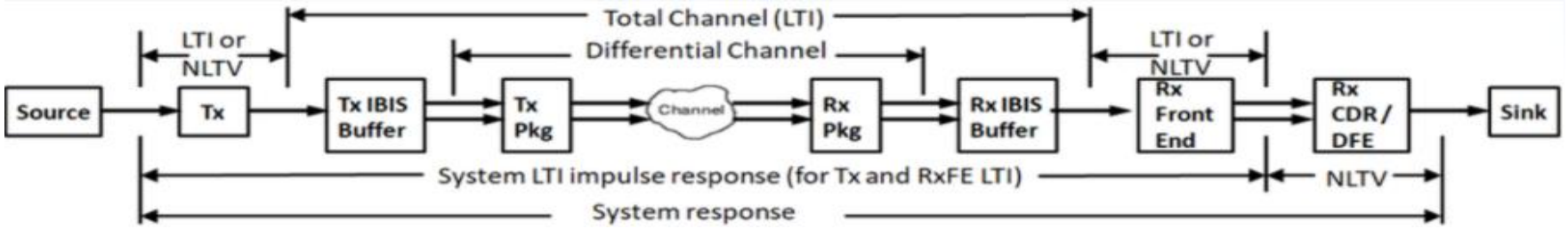


What is a SerDes Channel Simulator?

- A SerDes Channel Simulator combines frequency domain simulation, time domain simulation, DSP simulation and statistical simulation into one tool.
- Can quickly and accurately evaluate and optimize the SerDes system for performance.
- Enables evaluation of margin analysis, robustness of the design, verification of design implementation, and design tradeoffs.
- Before IBIS-AMI, SerDes system designers used traditional SPICE-based analysis.
  - Slow and could not simulate the millions of bits.
- With IBIS-AMI models and Channel Simulators, millions of bits can be simulated.
  - Effects of inter-symbol interference (ISI),
  - jitter (deterministic, Dj; Gaussian, Rj), and
  - cross-channel interference, and more.

Typical SerDes system line up in a Channel Simulator

- Source: NRZ or PAM4 data source
- Tx: Transmiter equalization; typically with an FFE.
- Tx/Rx IBIS Buffers: IBIS buffer to the differential channel; defines the on-die impedance.
- Tx/Rx Pkg: Package characteristic; typically defined with an SnP file.
- Channel: SerDes channel; typically defined with an SnP file.
- Rx Front End: Receiver equalization; typically with a CTLE.
- Rx CDR/DFE: Receiver timing/equalization; typically with a CDR and DFE.

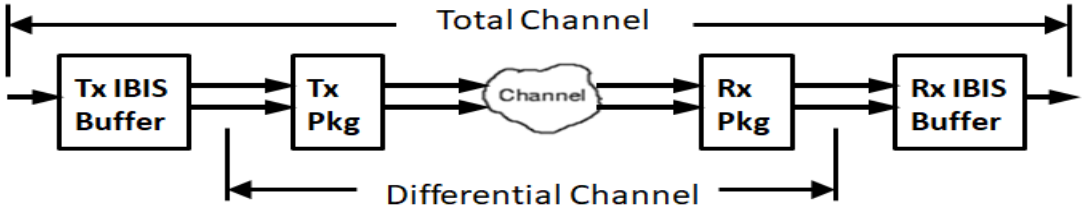


Channel Simulator Statistical Mode

- The full system is presumed to be LTI.
- No waveform analysis is performed; only the system impulse response is obtained.
- Step 1. The EDA tool obtains the impulse response for the full analog channel including the transmitter's analog output, the channel and the receiver's analog front end.
- Step 2. The Step 1 impulse is presented to the Tx AMI_Init function, the Tx model is executed, and the Tx model returns its modified impulse.
- Step 3. The Step 2 impulse is presented to the Rx AMI_Init function, the Rx model is executed, and the Rx model returns its modified impulse.
- Step 4. The EDA tool performs a statistical analysis of the Step 3 impulse to derive all eye density plot, eye metrics and BER plots.

Channel Impulse Response

- The total channel is represented in this block diagram.



- The differential channel often includes a Tx package and a Rx package.
  - This represents a hardware SerDes channel and is typically characterized by measuring its N-port S-parameters or obtained from a circuit simulator.
- The total channel is inclusive of the Tx IBIS Buffer and Rx IBIS Buffer.
- The total channel is converted to a single ended impulse inclusive of reflection mismatch and common-differential mode conversions.
  - The typical approach involves zero-padding the S-parameters and applying the constraints for physical realizability. This zero-padding approach often results in high frequency aliasing.
  - SerDesDesign.com uses a proprietary algorithm to obtain the causal channel impulse response which inherently does not result in any high frequency aliasing.

Channel Simulator Bit-by-Bit Mode

- Waveform analysis is performed; but only the output waveform statistics are collected - not the entire waveform.
- In this example, the Tx is LTI and the Rx is NLTV.
- Steps 1, 2 and 3 from the Statistical Model are performed.
- Step 4. The EDA tool produces a digital stimulus waveform; 0.5 when "high", -0.5 when "low", and may have a values between -0.5 and 0.5 where the Tx model *.ami file defines the timing jitter.
- Step 5: The Step 4 waveform is convolved with the Step 3 impulse.
- Step 6: The Step 5 waveform is presented to the Rx AMI_GetWave function which produces an output waveform. The model may also optionally return clock ticks marking the start of each UI.
- Step 7: The Step 6 outputs are used by the EDA tool to build a statistical histogram after the Rx model defined Ignore_Bits from which all EDA tools derive the eye density plot, eye metrics and BER plots.

IBIS-AMI model development challenges

- IBIS-AMI models and Channel Simulators have become an integral part of SerDes system design.
- SerDes vendors routinely provide IBIS-AMI models for their chips; often before the final chips.
- End users depend on high fidelity IBIS-AMI models and an accurate channel simulator to be able to predict their system behavior in their simulations.
- IBIS-AMI models are highly configurable.
- Model developers can design their models so that the equalization settings, adaptation loop parameters and corner cases can be chosen by the user.
- Key objective: IBIS-AMI models to accurately match the hardware performance in a real system.
- Therein lies the challenge.

Key decisions on the IBIS and AMI models

- Key decisions are required to convert Tx/Rx circuits into their IBIS-AMI representations.
- One can split the decisions as follows:

1) Partition the Tx/Rx design into a signal flow suitable for IBIS-AMI model representation.
   - This can be quite a challenging task and requires iterative discussion between the model developer and circuit developer to achieve a common understanding.

2) Provide the IBIS-AMI models with parameters that represent the Tx/Rx circuit control flow.
   - This task is to define all the states of the circuit to be represented in the model and define a set of parameters associated with each state.
   - Each state is represented with LTI and/or NLTV functionality by the model developer.

- The above decision process is not discussed in detail here.
- Tx/Rx IBIS buffer designs are assumed to properly represent the impedance loading the channel.