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Proposal for Automated EOE IBIS-AMI Modeling

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Abstract

Electrical-Optical-Electrical (EOE) systems typically represent repeaters and must be converted to IBIS-AMI models to be used in SerDes Channel Simulators. Today, the IBIS-AMI modeling process has matured so that the process can be automated. This allows the EOE device developer to extract data from their hardware for use in an IBIS-AMI model. Electrical characteristics can be captured with S-parameters or time domain waveforms. Optical characteristics, such as for highly nonlinear VCSEL devices, can be captured using optical instruments. This paper proposes a new methodology for automatically creating EOE IBIS-AMI Repeater Models based on EOE device measurements.

Authors Biography

John Baprawski is the Principal Engineer at SerDesDesign.com (www.serdesdesign.com) focused on modeling high speed digital (HSD) integrated circuits (ICs) based on the industry Input/Output Buffer Information Specification (IBIS) Algorithmic Model Interface (AMI) standard. He is the principal engineer and architect for the SerDesDesign.com web site, channel simulation, modeling tools and technology. For the past 10 years, he has provided custom NRZ/PAM4 Tx/Rx IBIS-AMI models and modeling training for over 40 high speed digital IC semiconductor companies. Prior to this consulting work, John was the R&D manager at Keysight Technologies EEsof Division for 22 years with responsibility for initiating and evolving their system level design tools including ADS Ptolemy, Wireless Libraries and SystemVue products. He holds a MSEE degree from University of California, Los Angeles, and PhD studies in Optical Signal Processing at University of Michigan.

Jocelyn Lebel a member of the Reflex Photonics engineering team for 3 years. He is responsible for IBIS-AMI models at Reflex Photonics. He previously worked for several years in systems engineering. He holds a MS in Physics and a BSEE from University of Sherbrooke.

Jon Burnett is a member of NXP Semiconductors' Board and Systems Solutions Team. He has worked in the PCB and System Signal Integrity field at the company (Motorola Semiconductors, Freescale Semiconductors, NXP Semiconductors) for 25 years. He has assisted in IBIS model generation and support, including co-authoring Motorola Semiconductor's first IBIS model in the mid-1990s. He holds a BSEE from Rice University.

1. Introduction

SerDes system design engineers are increasingly relying on Electrical-Optical-Electrical (EOE) devices, used as Repeaters, to meet their needs for systems operating at higher bit rates. Thus, they require IBIS-AMI behavioral models for the EOE Repeaters from various EOE vendors for use in Channel Simulators to evaluate their

system margins. They require high fidelity IBIS-AMI models that run very fast in Channel Simulators so that they can simulate tens of millions of bits to reveal system margin more accurately.

This in turn puts pressure on EOE device development engineers to provide IBIS-AMI models that are accurate and really represent their hardware. Developing such IBIS-AMI models is very challenging. The EOE developers must have expertise not only on their EOE device, but also device measurement skills (electrical and optical hardware instruments, circuit simulators), and software development skills (C++, Python, software build processes, Windows and Linux OS's, IBIS-AMI standard, and more).

Fortunately, the IBIS-AMI modeling process has matured so that today the process can be automated. The EOE device developer can focus on characterizing devices with "black box" stimulus/response measurements that capture the actual device performance.

New in this paper: Stimulus/response measurements for IBIS-AMI modeling include characterization of the VCSEL optical output waveform with an optical analyzer instrument using waveform averaging over a defined set of VCSEL bias levels and VCSEL modulation levels. Such optical waveforms capture the inherent VCSEL nonlinearity which includes different rise and fall times and characteristics.

New in this paper: A proposal for the EOE device modeling process is presented. The development steps, from the Electrical receiver, Optical components (driver/VCSEL/fiber/PIN/TIA), to Electrical transmitter, are illustrated. The combined "black box" stimulus/response data is used to automatically generate the EOE IBIS-AMI model which accurately represents the EOE device IP. Some modeling tradeoffs for accuracy and speed improvement are discussed.

2. Brief Overview of Optical E-O-E Repeaters

2.1 What are E-O-E repeaters

Electrical to Optical to Electrical (E-O-E) repeaters have been used for many years.

EOE repeaters are optical communications repeaters [1] used in a fiber-optic communications system to regenerate an optical signal. Such repeaters are used for many applications such as:

- extend the reach of optical communications links by overcoming loss due to attenuation of the optical fiber.

- replace electrical transmission to provide immunity to electromagnetic interferences, achieve longer reach, and achieve electrical isolation of TX and RX.

EOE repeaters are classified as:

- Redrivers: reamplification of the data pulse with pulse reshaping.
- Retimers: reamplification of the data pulse with retiming of the data pulse.

EOE repeaters provide superior bandwidth due to much lower loss than electrical channels and are promising candidates for data rates above 25G. Common to many EOE repeaters is the use of a VCSEL to emit photons. VCSEL stands for Vertical Cavity Surface Emitting Laser and is commonly used in Ethernet and in short reach applications.

Figure 2.1 show a typical optical link system using an EOE repeater [2].

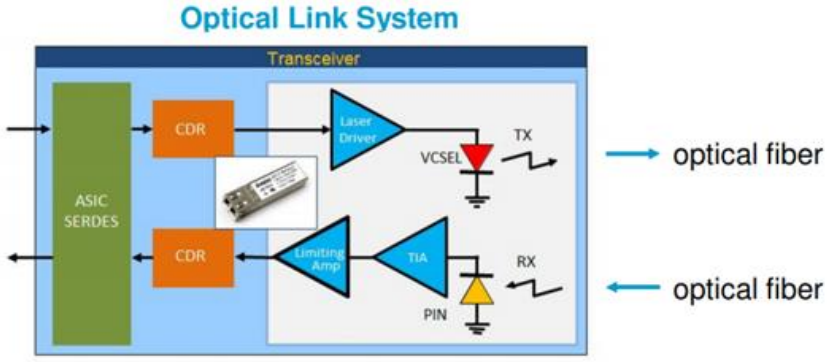


Figure 2.1: A typical optical link system

Inside the ASIC SERDES there is the Tx and Rx equalization and clock and data recovery.

Inside the optical module:

- The input current signal drives the vertical-cavity-surface-emitting laser (VCSEL) to emit photons.
- Photons propagate along the optical fiber.
- Photons are converted into photocurrent in the PIN diode.
- The transimpedance amplifier (TIA) converts the current into output voltage.

There are many companies creating EOE repeaters and systems. All contribute towards meeting the needs for the ever-increasing data speeds for data communications centers.

Figure 2.2 shows one example EOE repeater [3]: The Samtec Firefly system.

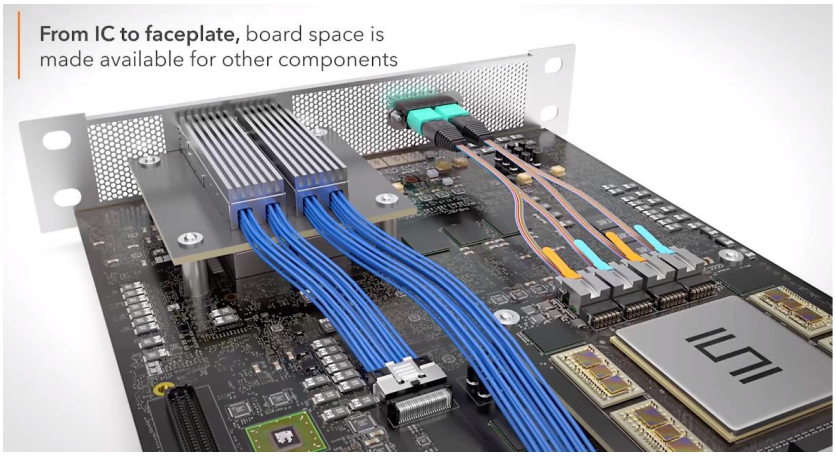


Figure 2.2: An example Samtec Firefly EOE repeater system

This example Samtec EOE system features high speed performance to 28 Gbps per channel with a path to 56 Gbps and with a miniature footprint to allow for extreme density to the ASIC module.

Figure 2.3 shows another example EOE repeater [4]. The Reflex Photonics (a division of Smiths Interconnect) Lightable system.

Figure 2.3: An example Reflex Photonics Lightable EOE repeater system

This example Reflex Photonics EOE system features up to 300 Gbps of full-duplex (12-lane 25 Gbps TRX) or 600 Gbps of half-duplex (24-channel 25 Gbps TX or RX) bandwidth data communication and can be used with FPGA front-end processing boards.

Figure 2.4 shows a typical block diagram for an EOE retimer used within a SerDes system.

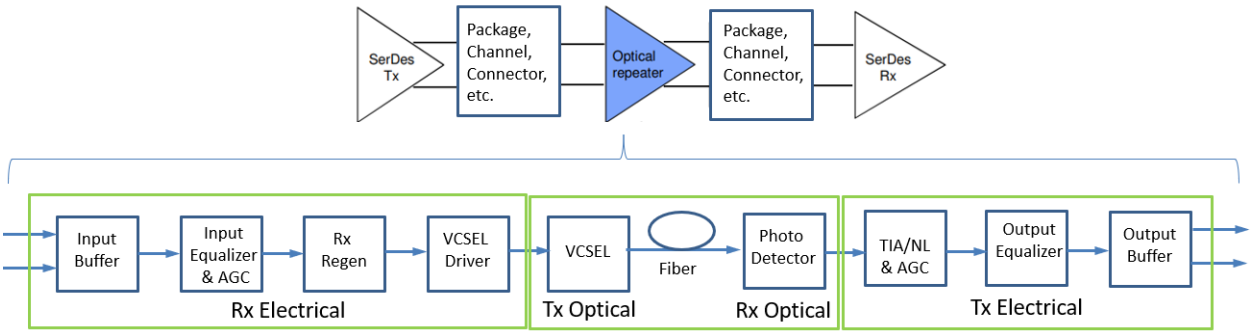


Figure 2.4: A typical block diagram for an EOE retimer

The receiver electrical section includes a differential channel input buffer, input channel equalizer and AGC, signal detector for signal regeneration, and a VCSEL driver.

The optical section includes the optical transmitter with VCSEL, optical fiber and optical receiver with PIN diode photo detector.

The transmitter electrical section includes a TIA with automatic gain control (AGC), nonlinearity, output channel equalizer and differential channel output buffer.

2.2 How are E-O-E repeaters used in system simulations

EOE repeaters are represented as IBIS-AMI models per the IBIS Open Forum standard [5].

Figure 2.5 shows a typical EOE repeater system to be simulated using the Keysight ADS Channel Simulator.

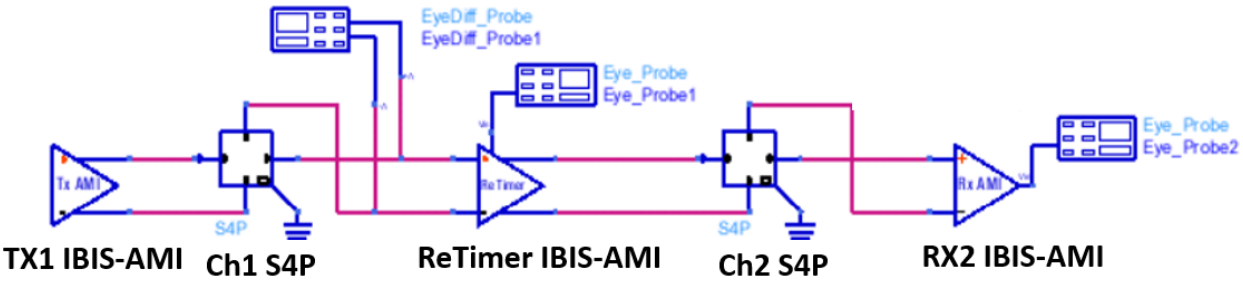


Figure 2.5: An example EOE repeater system in the Keysight ADS Channel Simulator

This figure shows a minimally configured repeater differential SerDes system with the cascade of 5 models:

- TX1 IBIS-AMI: which includes an AMI model followed by an output IBIS buffer.
  - For this discussion, the TX1 IBIS-AMI is linear and time invariant (LTI), but it can also be nonlinear and/or time variant (NLTV).
- Ch1 S4P: which is 4-port S-parameter file.

- ReTimer IBIS-AMI:
    - This IBIS-AMI model is actually a bundle of both an Rx IBIS-AMI at its input and a Tx IBIS-AMI at its output.
    - The input is a differential Rx IBIS portion,
    - The Rx AMI portion contains the input Rx equalizer, optical transmitter, optical channel and optical receiver,
    - This Rx AMI portion is NLTV.
    - The output of the Rx AMI portion has a tap for Channel Simulator display of its Waveform/Eye/BER performance,
    - The Tx AMI portion which contains the output equalizer,
        - For this discussion, the Tx AMI is LTI but can also be NLTV.
    - The output is the differential Tx IBIS portion.
- Ch2 S4P: which is a 4-port S-parameter file.
- RX2 IBIS-AMI: which includes an input IBIS buffer followed by an AMI model.

Both channels are defined with 4-port S-parameter files. Each channel may contain many parts which may be individually modeled. This includes the connectors, Printed Circuit Board (PCB) traces, vias, and package models to name a few.

For each channel, the total composite channel includes the Tx output IBIS buffer, the actual channel and the Rx input IBIS buffer.

The Channel Simulator assumes that this total channel is linear and time invariant (LTI). This enables the channel simulator to use fast simulation techniques to run millions of bits in a matter of minutes.

- Channel Simulation bit-by-bit mode is used (analogous to time domain simulation).
- Once the total channel has been characterized by the channel simulator, the transmitter's AMI model's effect on the channel is analyzed. The Channel Simulator provides the Tx AMI model the total channel impulse response; the Tx AMI model convolves its LTI impulse response with it to result in the Channel Simulator combined Tx+TotalChannel impulse response at the Rx AMI input.
- Then every bit (or PAM4 symbol) generated by Channel Simulator is convolved with this Rx AMI input impulse response to obtain the waveform into the Rx AMI model.
- The Rx AMI model is simulated with this waveform to generate its output waveform.
- The Rx AMI outputs available to the Channel Simulator are from the EOE repeater internal Rx AMI model and from the channel 2 final Rx AMI model.

For the output waveforms, the Channel Simulator builds a statistical amplitude histogram data base with 1 UI time-axis interval. At the end of the simulation, the Channel Simulator post processes this histogram data to derive the eye density plots, BER plots and other output metrics. This post processing can also include extrapolating the BER to lower levels than possible from a Monte Carlo type BER analysis.

The fast simulation speeds achieved with channel simulators, enables designers the ability to explore a large solution space comprising various model parameters and other system variables. This enables designers to have a much better understanding of how their system will perform under different conditions. [6][7][8]

3. Modeling the VCSEL module

The key process for modeling the EOE retimers discussed in this paper is to model the VCSEL module. The VCSEL module combines the VCSEL driver (voltage input and current output) and the VCSEL itself (current input and optical power output).

3.1 VCSEL module characteristics

The VCSEL is typically driven with a defined average current level (I-avg) with modulating peak-to-peak current level (I-mod) that switches between a high and low state.

In the logical High state, the laser is on and the current is defined by: $I_{high} = I_{avg} + I_{mod} / 2$

In the logical Low state, the laser is on and the current is defined by: $I_{low} = I_{avg} - I_{mod} / 2$

The relationship between drive current and optical power output for a VCSEL can be quite nonlinear as shown in Figure 3.1.

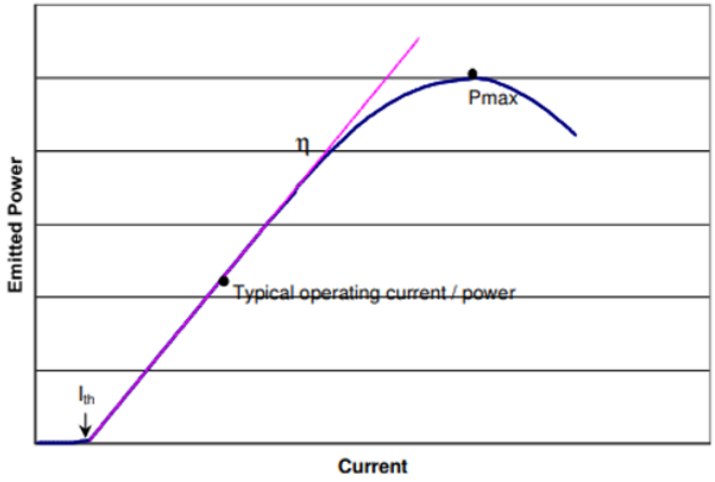


Figure 3.1: Typical VCSEL emitted power versus current

This figure shows that the VCSEL emitted power begins above a threshold current, has a peak power, and has a linear current to optical conversion efficiency. The operating point, I-avg, is typically in the linear region. This figure does not adequately represent the VCSEL

characteristic. The VCSEL is very nonlinear and has different characteristics for its rising waveform and falling waveforms.

More detailed VCSEL module characteristics were measured by Reflex Photonics. Using a Reflex Photonics Lightable EOE retimer, time domain waveforms for the VCSEL module output optical power were collected for various I-avg and I-mod values. The bit rate of 10.3125 Gbps was used with repeating NRZ data pattern of 10 0's and 10 1's. The Keysight N1090A scope was used with waveform averaging set to 256. The data collected from the scope includes the noise level detected in the waveform.

Figure 3.2 shows the VCSEL optical output power for test case with I-avg = 6.9 mA and with I-mod varied over the range {0.4, 0.8, 1.7, 3.3, 5.0, 6.7, 8.5, 10.0} mA.

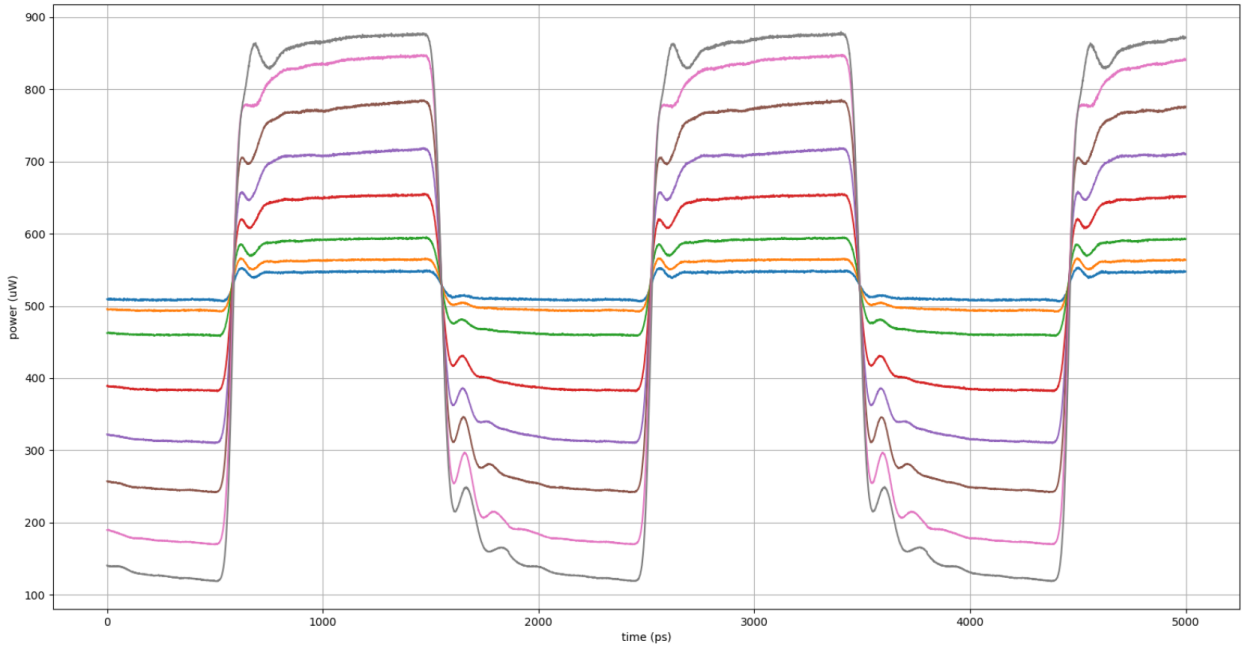


Figure 3.2: Reflex Photonics VCSEL output power vs modulation current settings

This figure shows the more detailed nonlinear characteristics of the VCSEL output power for a fixed operating average current level, I-avg, as the modulating current level, I-mod, is varied. The bit rate is 10.3125 Gbps bit rate with a repeating pattern of 10 1's and 10 0's. Observe the typical VCSEL nonlinearity with the different rising and falling waveform patterns as the I-mod level is changed. Each rising and falling transient has a duration over several UI's. The VCSEL output has a noise level that is larger relative to the modulation level when the I-mod level is lower. The highest signal to noise ratio occurs when I-mod is larger.

3.2 Possible approaches for modeling the VCSEL module

There are many approaches used in the industry to model VCSEL modules. Some of which are listed here:

- Simple nonlinear model based only on the optical output power versus drive current shown in Figure 3.1.
- Keysight Physics-Based VCSEL Model introduced in 2014 [10].
- VPI Photonics software for modeling photonic systems [11].
- Keysight Electrical-Optical-Electrical System Design Workflow which integrates the VPI Optical Link [12].

3.3 Approach taken for modeling the VCSEL module

In this EOE retimer modeling example, the VCSEL module was treated as a "black box" with stimulus/response waveforms used to define its characteristics. The VCSEL module was based on the data collected by the optical scope as shown in Figure 3.2. The measured VCSEL characteristics were provided by Reflex Photonics.

With this approach, the VCSEL model is setup as a time varying filter. The input data includes sets of characteristics shown in Figure 3.2 for various I-avg and I-mod levels. The model performs a multi-dimensional interpolation on the data to derive the characteristics for any specified I-avg/I-mod levels used. The model is time varying and changes for every simulation time increment.

A VCSEL model based on measured VCSEL characteristics inherently gives an exact match to the modeling data.

3.4 Additional features desired in the VCSEL model

Such a hardware based VCSEL model can include additional features.

- The VCSEL model can resample its data for any new SymbolRate or SamplesPerSymbol used during Channel Simulation.
- The VCSEL model can optionally apply additional AWGN noise (such as the noise level as reported by the scope during the measurement gathering).
- The VCSEL model can optionally include driver current peaking with 1 or more peaking steps to compensate for the ISI in the rising and falling waveforms independently.
    - This peaking compensation can be automatically optimized by the model.
- The VCSEL model can remove its output common-mode level for easier use with a Channel Simulator which ignores any common-model levels.
    - The common-mode compensation can be optimally set by the model which can be different for different VCSEL settings and data pattern.

The VCSEL compensation current peaking process used here is based on the process reported in the industry by C. Yang et. Al in 2014 [9].

For the VCSEL test case with I-avg = 6.9 mA and I-mod = 5.0 mA, the VCSEL model used a 5-step compensation to automatically determine the optimal compensating driver current pulses for the rising and falling waveform responses. These rising and falling current waveforms are overlaid on the optical output power waveform in figure 3.3 using a repeating waveform of ten 1's and ten 0's.

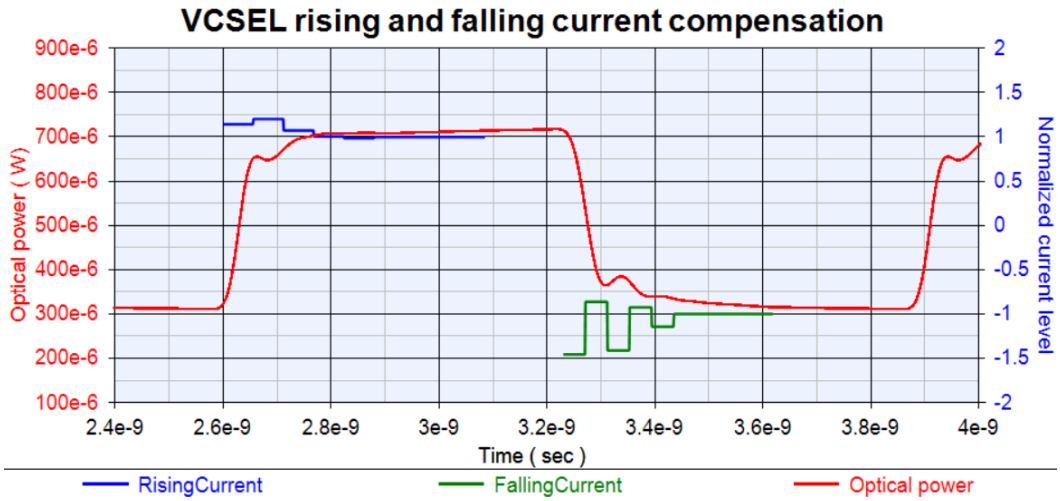


Figure 3.3: VCSEL compensation currents for rising and falling waveforms.

In this figure, the bit rate is 10.3125 Gbps bit rate with a repeating pattern of 8 1's and 8 0's. The optical power axis is on the right. The normalized current axis is on the left. The rising and falling currents are normalized to the 5.0 mA modulation current level. The optical output power has average power bias = 514 uW and nominal peak to peak modulation power = 406 uW. The optimized rising edge has a current peaking pulse width = 0.58 UI and five compensation peaking ratios = 1.14427, 1.20239, 1.07387, 1.00667 and 0.986905. The optimized falling edge has a current peaking pulse width = 0.67 UI and five compensation peaking ratios = 1.45677, 0.862242, 1.41073, 0.924318 and 1.14222.

Figure 3.4 shows the VCSEL output power waveform without and with peaking compensation using a repeating waveform of 8 1's and 8 0's.

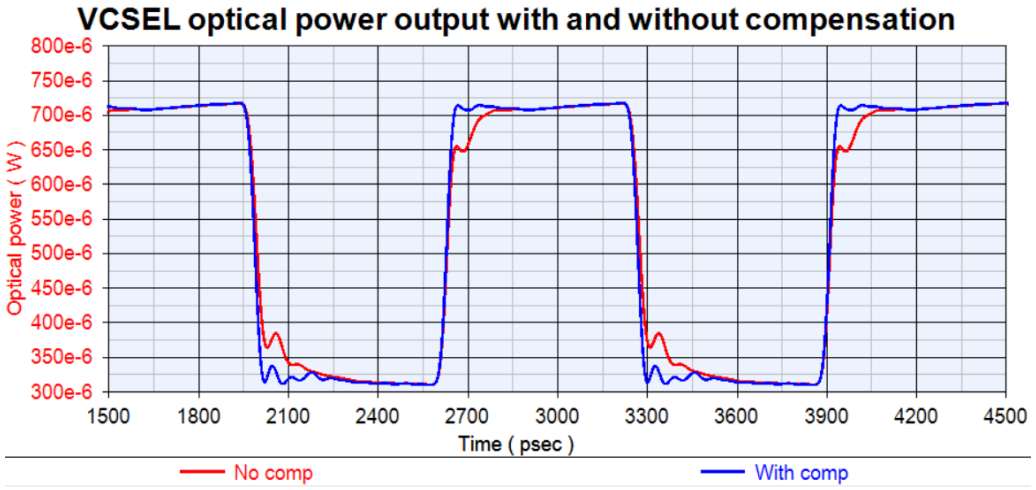


Figure 3.4: VCSEL output power without (red) and with (blue) peaking compensation.

As can be seen, the peaking compensation corrects the distortions in the VCSEL rising and falling waveforms.

Figure 3.5 shows the VCSEL output power eye over 2 UIs without and with peaking compensation using a PRBS 10 data pattern.

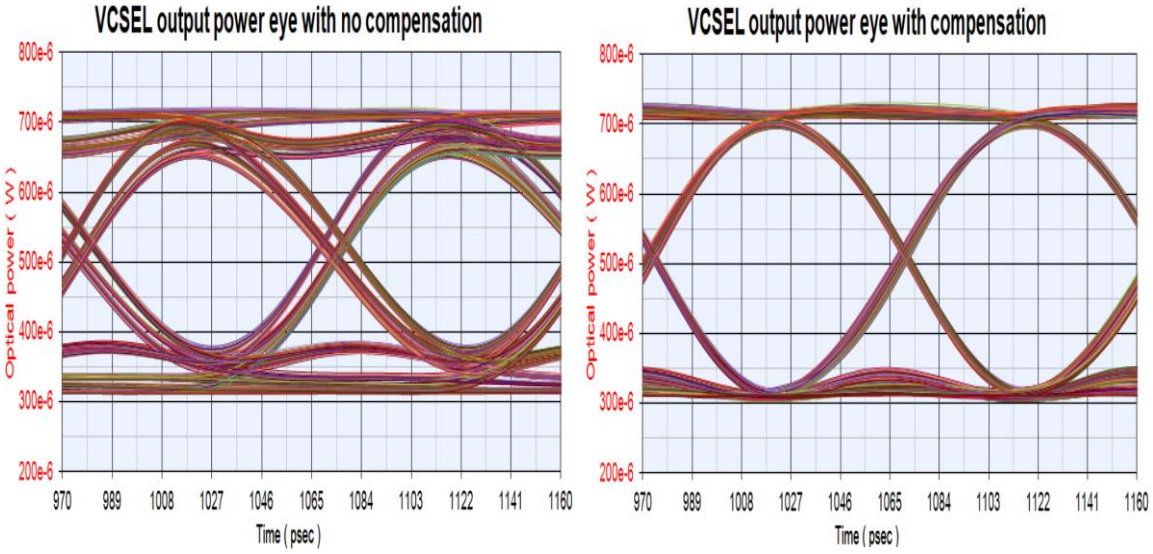


Figure 3.5: VCSEL output eye without (left) and with (right) peaking compensation.

As can be seen, by using the peaking compensation in the VCSEL module, the VCSEL output eye has suppressed jitter and the eye-opening height is also near-perfect.

4. Proposal for EOE IBIS AMI Model Development

The EOE retimer IBIS-AMI model development process discussed here is a proposal. No specific EOE retimer has been developed per the proposal discussed. Various parts of the EOE retimer example have been developed in context with various separate development projects. This paper pulls the various pre-existing modeling processes together to propose the current EOE retimer development process.

The target EOE retimer has the block diagram shown earlier and reshown here in Figure 4.1.

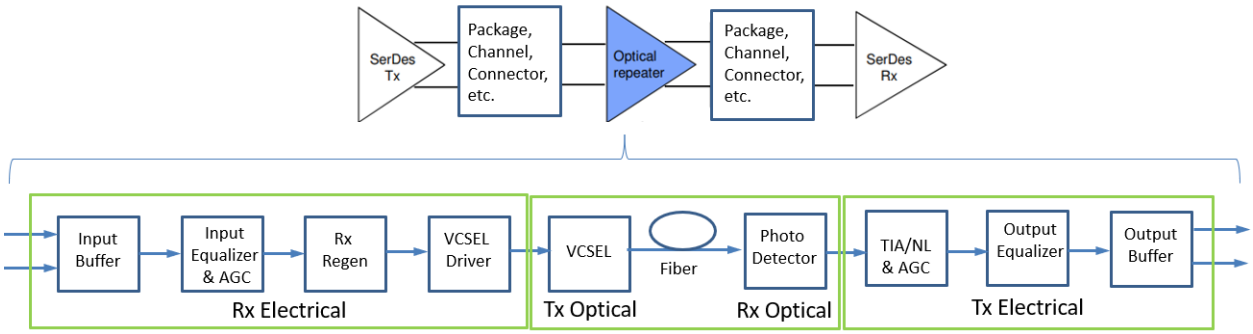


Figure 4.1: A typical block diagram for an EOE retimer

Throughout the example, reliance is made on stimulus/response measurements (using hardware or circuit simulations) in the time domain or frequency domain to record circuit characteristics for the various blocks in this block diagram. It is assumed that any hardware measurements include the de-embedding of test fixture characteristics so that the characteristics collected are only based on the circuit as desired.

There can be many possibilities for the configuration of this EOE retimer. There can be many corner cases. There can be many different states for any of the blocks. There can be a range of bit rates, with possible sub-ranges defined. For such possibilities, data would be collected over all configurations.

The discussion to follow limits the variables to those discussed. However, the process can accommodate any variations on the configurations and states.

4.1 Modeling the IBIS buffers

In this EOE example, the IBIS buffers were based on the use of measured S-parameters. The Tx and Rx IBIS Buffer four port S-parameters were provided by NXP Semiconductor.

The options for modeling the IBIS buffer, prior to the IBIS 7.0 standard, was limited to various simplistic RLC type circuit configurations. With IBIS 7.0, the IBIS buffer can now

be modeled using S-parameters. Per the standard, four port S-parameters are used for modeling the IBIS buffer interface to the differential channel.

IBIS buffer models based on measured S-parameters provides a higher fidelity IBIS model, especially when the actual circuit characteristics do not really match the limited IBIS RLC circuit options.

4.2 Modeling the Rx Input Equalizer

In this EOE example, the Rx input equalizer was based on the use of measured equalizer step response characteristics provided by NXP Semiconductor.

The Rx equalizer purpose is to compensate the waveform at the Channel 1 output and open the eye before the Rx Regeneration model. The Rx equalizer is defined with a Feed-Forward-Equalizer (FFE).

This FFE design was provided by NXP Semiconductor and is a 3 tap FFE used for bit rates from 1.0 Gbps to 28.05 Gbps and used with three corner cases. For each corner case, there are:

- 14 Drive level states
- 25 PreCursor states (12 negative, 0, 12 positive)
- 33 PostCursor states (16 negative, 0, 16 positive).

The FFE was treated as a “black box” with stimulus/response waveforms used to define its characteristics. The modeling approach relies on characterizing a reduced set of states but still supports the full set of states by use of data interpolation and gain scaling as determined by the model.

Since the FFE characterization waveforms inherently included the IBIS buffer, the IBIS buffer characteristics must be de-embedded from the from the FFE waveform data to achieve the AMI model. Fortunately, the FFE model can automatically de-embed the IBIS characteristic.

Figure 4.2 shows the FFE step response waveforms for a fixed Drive and fixed PostCursor as the PreCursor is varied over 13 states.

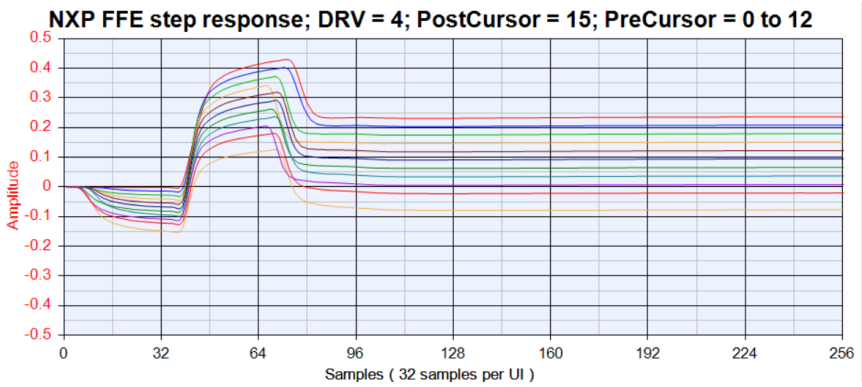


Figure 4.2: FFE step response waveforms

During simulation, the FFE model automatically resamples the FFE step response data and de-constructs the FFE data to derive the FFE tap gains (G1, G2, G3) and FFE filters (F1, F2, F3) for use in the AMI simulation as shown in Figure 4.3.

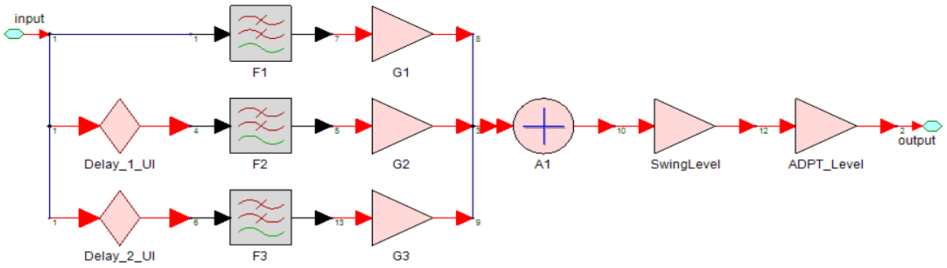


Figure 4.3: FFE de-construction model for the FFE step response data

An FFE model based on measured FFE characteristics inherently gives an exact match to the modeling data.

4.3 Modeling the Rx Regenerator

In this EOE example, the Rx regenerator was modeled based on the defined clock-and-data-recovery (CDR) observed-jitter-transfer-function (OJTF) characteristic.

This CDR is based on an industry standard bang-bang phase detector approach.

The phase detector detects data transitions and data states to determine whether the CDR clock is early or late and adjusts the CDR clock timing accordingly. This phase detector is strongly nonlinear and does not have a simple theoretical analysis.

The phase response of a system which uses a CDR to generate its reference clock is the observed jitter transfer function, OJTF, which is related to the JTF in the frequency domain as OJTF(f) = 1 - JTF(f) (phase matters).

The OJTF has a high pass frequency response. Jitter significantly below the corner frequency, OJTF Fc, is not observed. OTJF gives the amount of jitter which is tracked and therefore not observed at the output of the CDR as a function of the jitter rate applied to the input. OJTF is typically the quantity measured when evaluating the CDR jitter characteristic. Using a bit rate of 25 Gbps, Figure 4.4 shows the measured OJTF for the CDR with a 15 MHz OJTF corner frequency value.

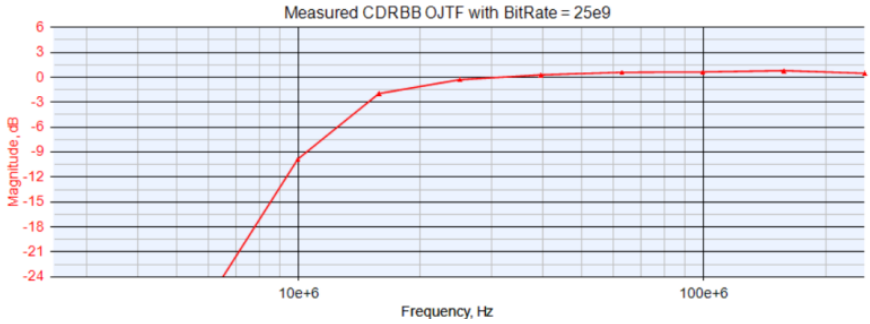


Figure 4.4: CDR Observed Jitter Transfer Function with a 15 MHz corner frequency

A CDR model based on measured OJTF Fc characteristic gives a reasonable representation of the actual circuit performance.

4.4 Modeling the optical fiber, optical detector and TIA/NL

In this EOE example, the optical fiber, optical detector and TIA with nonlinearity were modeled using algorithmic models as well as measured small and large signal characteristics.

The optical fiber model used has these settable parameters:

- FiberLoss = Optical cable loss per unit length in dB/km.
- FiberLength = Optical cable length in meters.
- FiberConnectorLoss = Optical cable connector loss in dB.
- FiberCouplingLoss = Optical cable coupling loss in dB.
- FiberLossBW = Optical cable bandwidth-loss product (GHz * m)

The optical detector and TIA used has these settable parameters:

- Responsitivity = Photo-diode responsitivity, mA / mW
- PD_Capacitance = Photo-diode capacitance, uF.
- TIA_Resistance = Trans-impedance resistance, V / A. This capacitance and resistance results in a low pass filter (RC time constant) at the photodiode output.
- EnableAGC = option to enable an automatic gain control at the TIA output.
- AGC_Level = Target peak-to-peak eye level.

The TIA nonlinearity is defined from its small and large signal characteristics. This small and large signal data was provided by NXP Semiconductor.

The nonlinearity small signal characteristic is defined with its step response as shown in Figure 4.5 with gain versus time.

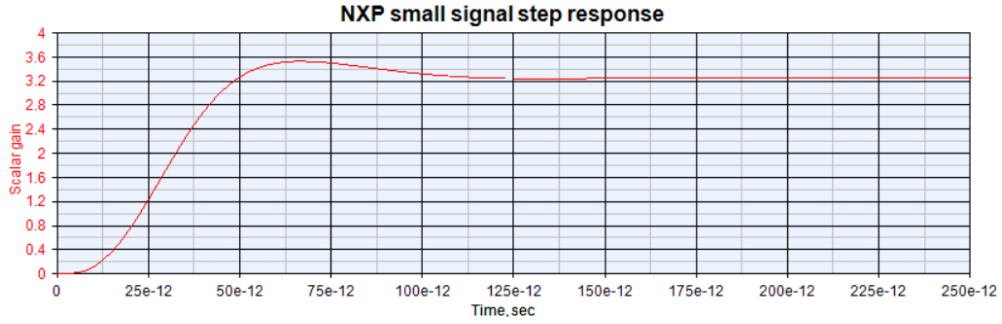


Figure 4.5: Nonlinearity small signal step response

The nonlinearity large signal characteristic is defined with its swept input/output level response as shown in Figure 4.6 with output level versus input level.

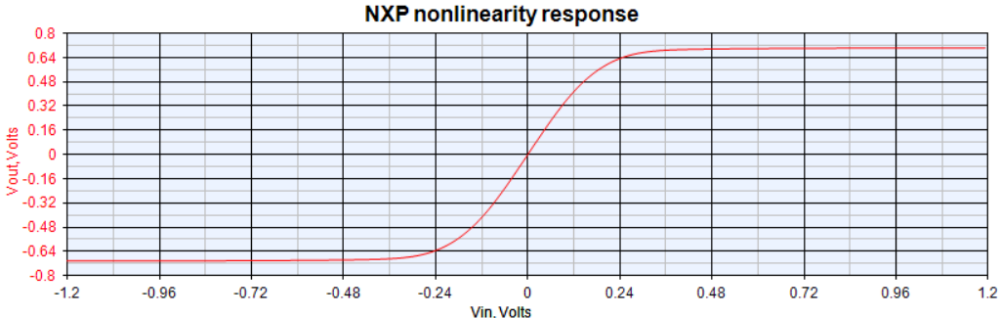


Figure 4.6: Nonlinearity large signal swept level response

A nonlinearity based on the measured small and large signal characteristic gives a reasonable representation for the actual circuit performance.

4.5 Modeling the Tx Output Equalizer

The purpose of the Tx equalizer is to apply pre-emphasis to the output waveform to compensate for the waveform at the Channel 2 output.

In this EOE example, the Tx output equalizer was based on a multi-tap FFE with output filter. The number of FFE pre and post cursor taps can be selected. The FFE can automatically select the optimal FFE tap values to optimize the Channel 2 output eye opening.

5. Automated EOE IBIS-AMI model generation

5.1 Using the modeling data

The EOE retimer modeling data discussed in the prior section needs to be combined into one IBIS-AMI model.

To do this, a Channel Simulator was used with models that readily accept characterization data from circuit simulations or hardware measurements. The EOE SerDes system was setup up using a series of blocks represented in Figure 5.1.

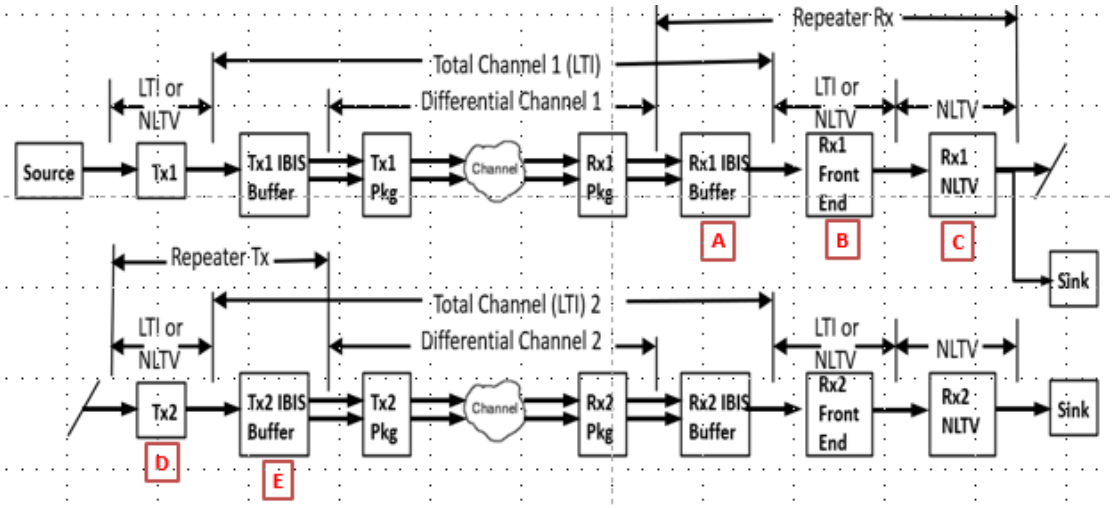


Figure 5.1: SerDes EOE repeater system blocks

As shown in this figure, the repeater is the interface between an input channel 1 and an output channel 2. Each block in the total channel (Tx IBIS buffer, Tx package, channel, Rx package and Rx IBIS buffer) can be represented with S-parameters. The Repeater Rx section has more detail in its Rx1 NLTV block to represent the optical transmitter, optical channel and optical receiver.

Each of these blocks are configured for the EOE Repeater SerDes system. Data files discussed in the prior sections are uploaded for modeling the EOE Repeater with these sections:

- A: Rx Input IBIS buffer: S-parameter data
- B: Rx Input Equalizer: Waveform data
- C: VCSEL and driver: Waveform data
- D: TIA nonlinearity: Small-signal waveform data and large signal nonlinearity data
- E: Tx Output IBIS buffer: S-parameter data

Once the complete SerDes system and EOE retimer has been setup, many simulations can be run to explore the SerDes system design space for this EOE retimer. Thousands or millions of UIs can be simulated quickly and displays can be opened to observe Waveforms, Eye Density plots, BER Waterfall curves and other eye metrics.

For this EOE example, the BitRate is 10.3125 Gbps with 32 samples per bit. Bit-by-bit mode is used with 100,000 UIs. The EOE input Rx equalizer is setup to automatically set its states to optimally equalize its output inclusive of the Total Channel 1 roll-off. This Rx equalizer also includes an AGC to achieve the target output eye peak-to-peak level. The EOE VCSEL is set up to automatically set its current driver pulse states for optimal VCSEL rise and fall waveform compensation and for removal of the VCSEL output common-mode level. The EOE PIN/TIA is set up to automatically achieve its output target AGC level.

For this discussion, the focus is on the repeater TIA output. The Total Channel 1 is inclusive of the characteristics for the Tx 1 IBIS buffer (which in this example is defined with an ideal differential 100 Ohms) and the repeater Rx IBIS input buffer (which in this example is defined with an S4P file). Figure 5.2 shows the Total Channel 1 response characteristic in the frequency domain.

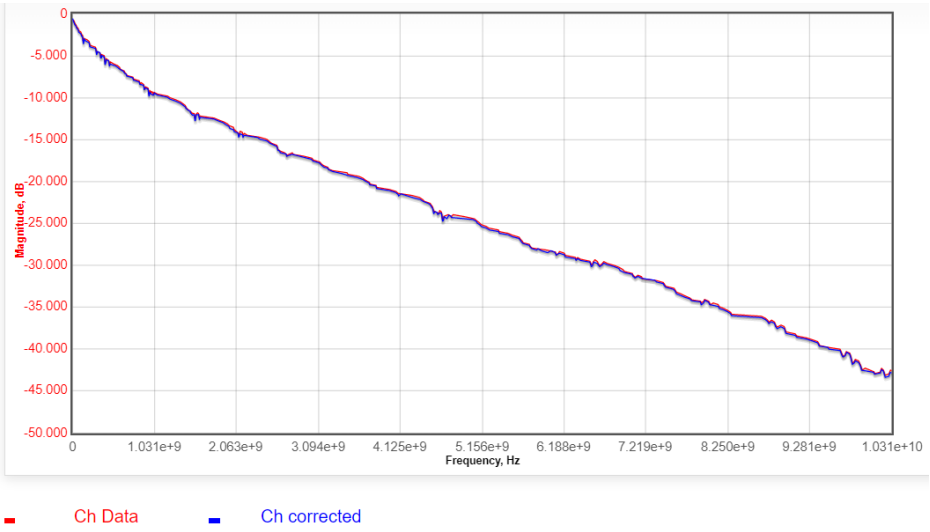


Figure 5.2: Total Channel 1 Impulse Response in the frequency domain

In this figure, the Total Channel 1 raw data differential characteristic in the frequency domain is RED. This data is based on differential S-parameters and circuit analysis in the frequency domain. As such, the data is inherently frequency band limited and non-causal in the time domain. It requires corrections for proper representation with a time domain impulse response. Once that data to impulse conversion is made, the impulse can then also be represented in the frequency domain. In this figure, the impulse response in the frequency domain is BLUE. The impulse response shows accurate tracking of the Total

Channel 1 data differential characteristic. Total Channel 1 has about 25 dB loss at Nyquist. With this loss, the Total Channel 1 output eye is completely closed.

The Rx 1 Equalizer is run with its states automatically set to optimally open its output eye. Figure 5.3 shows the eye density plot at the output of the Rx 1 Equalizer.

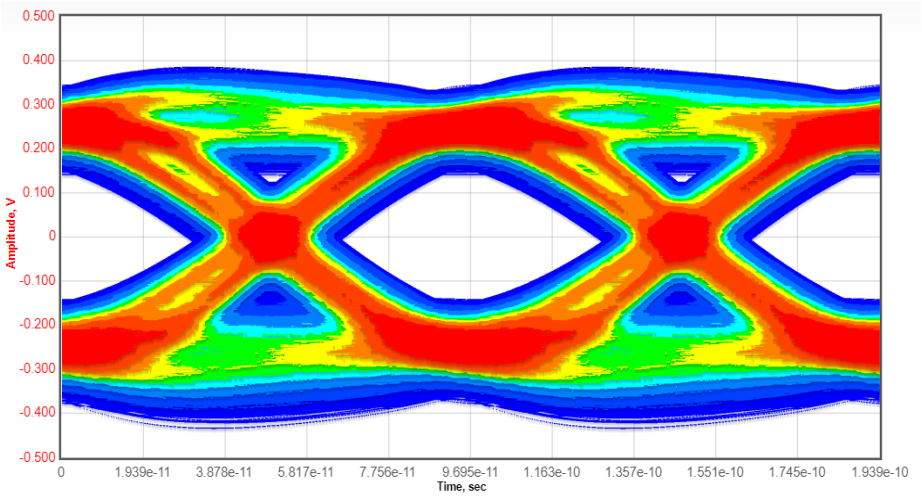
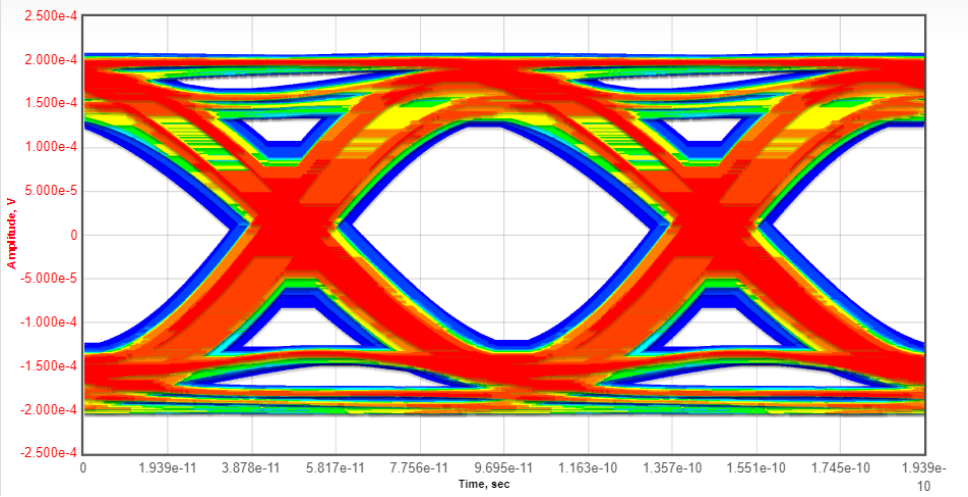


Figure 5.3: Eye Density plot at the Rx Input Equalizer output

In this figure, the output of the repeater Rx input equalizer is seen to have an open eye and its AGC action has set the single sided eye level to the target 0.25 Volt level.

Figure 5.4 shows the eye density plot at the output at the VCSEL output (without compensation) and PIN/TIA output (with VCSEL compensation and AGC).



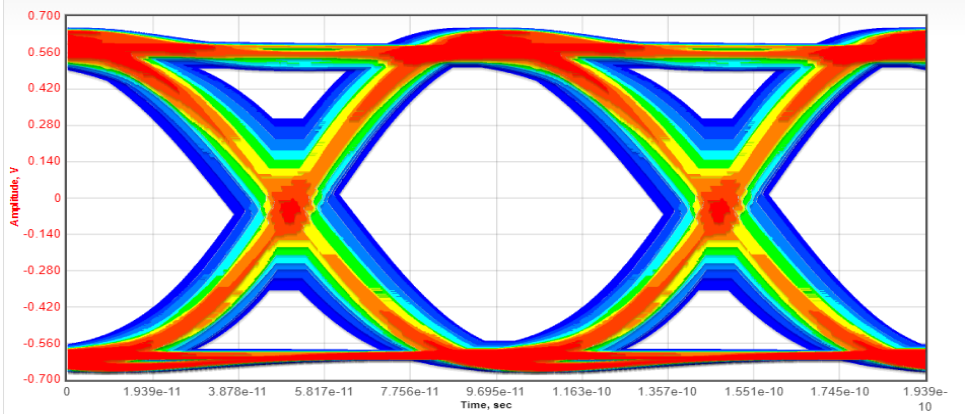


Figure 5.4: Eye Density plots; VCSEL output (no compensation, upper), PIN/TIA output (with VCSEL compensation, lower)

As can be seen in this figure the VCSEL compensation reduces the timing jitter and opens the eye height.

Many simulations were run to verify proper EOE retimer model operation and performance.

5.2 Generating the IBIS-AMI model

After one has explored the EOE SerDes system design space to satisfaction, it is time to generate the EOE retimer IBIS-AMI model.

To do this, one enables the Channel Simulator analysis setup parameter GenerateModels and rerun a simulation.

Once this is done, the IBIS-AMI model files are generated at the end of the simulation. The generated model can include any additional instructions for the model, such as actual desired model name and parameter names for example.

The generated IBIS-AMI model files include all the relevant *.ibs, *.ami, *_x64.dll (Windows) and *_x64.so (Linux) files.

The Windows/Linux build projects for the generated IBIS-AMI model can be provided with source code so that any part of the included data can be changed as needed to change the existing EOE IBIS-AMI model or create new EOE IBIS-AMI models.

6. Testing the IBIS-AMI EOE model

The EOE retimer IBIS-AMI model can now be used in any Channel Simulator. The model generated in the prior step is named EOE_Repeater and is used two Channel Simulators: 1) the Channel Simulator A which contains the automated EOE IBIS-AMI modeling and 2) Channel Simulator B which is another popular in the industry.

For use in a Channel Simulator, and per the IBIS-AMI standard, this IBIS-AMI model must be identified as a repeater type called ‘redriver’ (not ‘retimer’) because there is not to be any NRZ regeneration by the Channel Simulator at the output of the EOE_Repeater Rx section. The EOE Rx section internally does the NRZ regeneration before the internal VCSEL model.

For this report, the SerDes system settings are the same as in the prior section. The bit rate is 10.3125 Gbps with 100,000 UIs simulated in Bit-by-Bit mode.

The Channel Simulator A EOE IBIS-AMI TIA output eye density is shown in Figure 6.1.

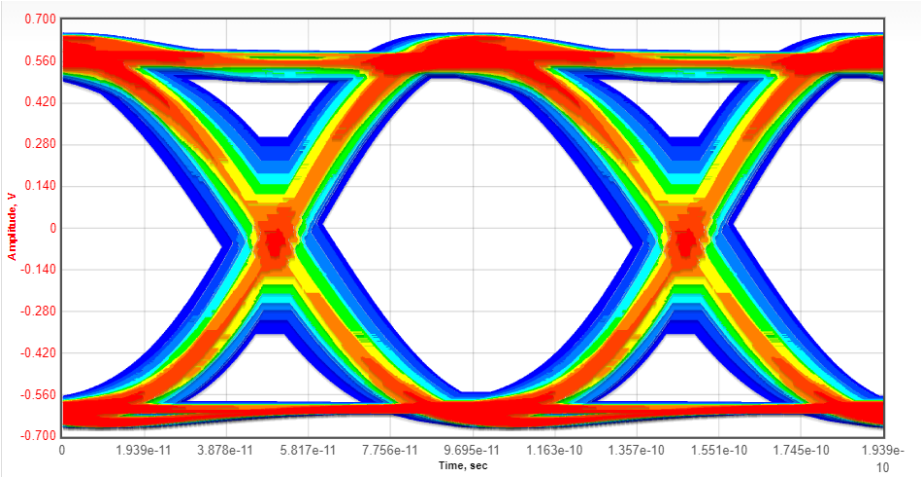


Figure 6.1: Channel Simulator A EOE output eye density plot.

This IBIS-AMI output eye density is the same as measured using the individual components during the model development shown in Figure 5.4 (lower).

The Channel Simulator B schematic display is shown in Figure 6.2.

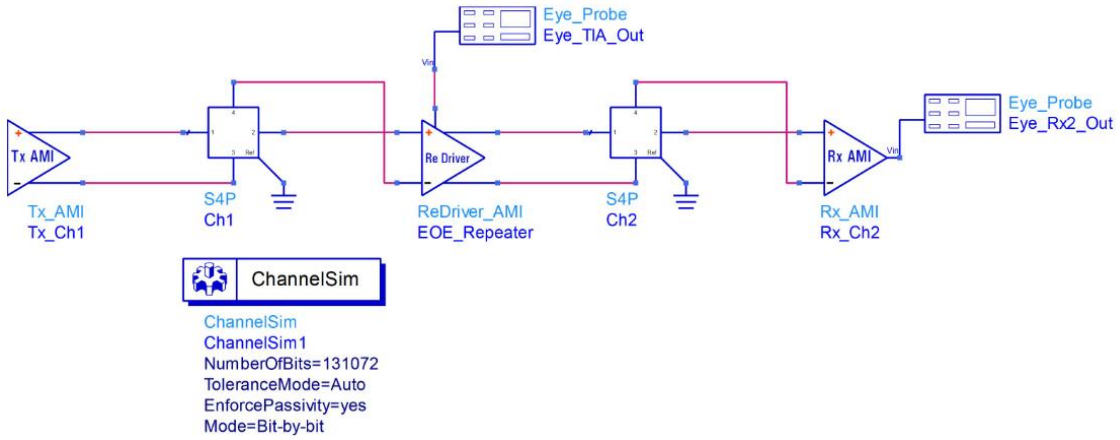


Figure 6.2: Channel Simulator B EOE Repeater schematic.

The Channel Simulator B display for the EOE IBIS-AMI TIA output eye density is shown in Figure 6.3.

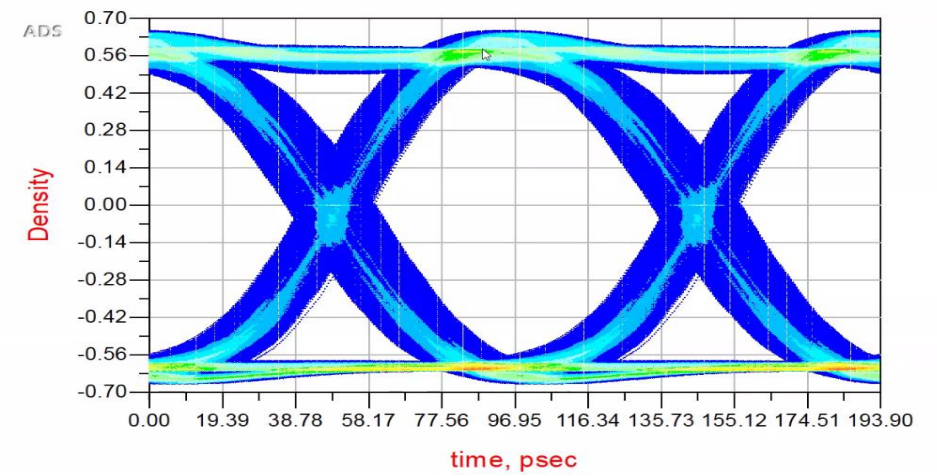


Figure 6.3: Channel Simulator B EOE output eye density plot.

As can be seen, this 'B' eye density plot is essentially the same as that from 'A' with differences in the eye density coloring. The automatically generated EOE model is portable among different Channel Simulators that conform to the IBIS-AMI standard.

7. Engineering Trade-offs

The EOE retimer modeling steps taken in this paper can be modified to trade off accuracy and speed.

The approach taken for the VCSEL module inherently has high accuracy based on the use of hardware measured waveforms for various VCSEL driver I-avg and I-mod settings. The VCSEL model inherently has fast speed. The VCSEL model can be improved with better and more detailed hardware measurements.

The approach taken for the Rx Equalizer inherently has high accuracy based on the use of detailed circuit simulation waveforms. Since the Rx IBIS characteristic is automatically de-embedded from the waveform data, the Rx Equalizer AMI model has high accuracy. The Rx Equalizer model can be improved with better and more detailed circuit measurements.

The use of four port S-parameter data to represent the IBIS buffers inherently has high accuracy. The accuracy can be improved with better and more detailed S-parameter measurements. However, the S-parameter accuracy is often compromised when used with a Channel Simulator since each Channel Simulator must convert S-parameters to a time domain representation. Whenever S-parameters are used, comparisons must be made between the S-parameter data differential characteristic and its impulse representation in the frequency domain to discern the accuracy of the S-parameters impulse representation.

Fortunately, Channel Simulator A provides such comparisons for easy evaluation of the accuracy of its impulse characterizations and has a proven track record for impulse modeling accuracy.

The approach taken for the optical fiber and optical detector were based on a simplified parameterized algorithmic model. These models can be improved to consider more physical effects.

8. Conclusions

This paper presented a proposal for automating the generation of IBIS-AMI models for Electrical-Optical-Electrical repeaters. In such repeaters, the VCSEL to be modeled presents a challenge since it is highly nonlinear and has differing rising and falling waveforms. This paper shows that it is practical to use VCSEL hardware waveform measurements from an optical scope to accurately represent the VCSEL module which includes the VCSEL current driver. Besides the VCSEL module, an EOE repeater has many more modules for equalization, pulse regeneration, optical channel and optical receiver. The EOE device developer can focus on characterizing devices with "black box" stimulus/response measurements that capture the actual device performance. The VCSEL “black box” measurements are over a defined set of VCSEL bias levels and VCSEL modulation levels. This paper has shown that collecting the characteristics for all components in an EOE repeater can be readily achieved and consolidated into one model. The combined “black box” stimulus/response data are used in an automated EOE IBIS-AMI model generation process which accurately represents the EOE device IP. Using this approach, EOE repeater IBIS-AMI models can be easily explored with different sets of data for accuracy and speed trade-offs with automated IBIS-AMI model generation achieved once one is satisfied with the SerDes system simulation results for the EOE repeater model.

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